Effect of forming gas annealing on the degradation properties of Ge-based MOS stacks

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1. Abstract

The influence of forming gas annealing on the degradation at constant stress voltage of multi-layered germanium-based Metal-Oxide-Semiconductor capacitors (p-Ge/GeO_x/Al_2O_3/High-K/Metal Gate) has been analyzed in terms of the C-V hysteresis and flat band voltage as function of both negative and positive stress fields. Significant differences were found for the case of negative voltage stress between the annealed and non-annealed samples, independently of the stressing time. It was found that the hole trapping effect decreases in the case of the forming gas annealed samples, indicating strong passivation of defects with energies close to the valence band existing in the oxide-semiconductor interface during the forming gas annealing. Finally, a comparison between the degradation dynamics of Germanium and III-V (n-InGaAs) MOS stacks is presented to summarize the main challenges in the integration of reliable Ge – III-V hybrid devices.

2. Introduction

As the physical dimensions of transistors scale down, the velocity saturation of carriers in the MOSFET channel (mainly caused by optical phonon emission[1]) has become a limiting factor in

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performance[2]–[4]. Inducing strain in the Si channel has been the approach to overcome this issue and enhance mobility in current Si-based CMOS processes, as it alters the band structure of the channel, increasing the occupancy of the low effective mass valley and then the mobility [5].But it has been a short-term solution [3]. For keeping the pace of increase in the number of devices per chip, a paradigm shift is required, which considers the emergence of new channel materials, as it is defined in the International Technology Roadmap of Semiconductors (ITRS) goals [6].

Aiming to fulfill this requirement, materials with high-carrier-mobility and therefore improved injection velocity such as Germanium (Ge) – up to 4 times larger bulk mobility for holes respect to Silicon [7] - and III-V compounds (such as InGaAs) -up to 2 times larger bulk mobility for electrons have been proposed as possible candidates to replace Silicon as channel material[3], a key step in the development of high-performance P and N MOS transistors, respectively[3], [8]. Furthermore, dense 2D integration of InGaAs and Ge has been recently shown on a Si substrate[9] (Ge – III-V Hybrid Technology), utilizing standard CMOS processes. InGaAs nFETs and SiGe pFETs have been reported down to 25 nm spacing, along with inverters and dense SRAM cells implemented with finFETs. This novel and scalable CMOS integration scheme enables InGaAs nFET fabrication in close proximity to Ge-pFETs. In this context, it is relevant to understand the limiting factors of the Ge- and InGaAs-based MOS stacks, given the various types of defects that degrade their performance and seriously impact their reliability[10]–[12]. Therefore, the implementation of new materials in actual devices requires the capability of predicting and minimizing the long-term degradation as well as the impact of process changes on the degradation phenomena.

Regarding InGaAs, much progress has been made in the passivation of charge trapping defects in the Al_2O_3/InGaAs gate stacks, including traps at the oxide/III-V interface[13]–[16]. Nevertheless, it has been shown[17], [18] that despite of the improvement in the interface quality in terms of the passivation of both border traps (BT) and interface states (D_{it})[16] (by suppression of Ga-O bonds), surface treatment with NH_4OH and Forming Gas Annealing (FGA) (H_2/N_2)contribute to the generation of charge in the dielectric layer by dissociation (i.e., depassivation) of the bonds at the interface[17] when a stressing voltage is applied. This causes a significant increase of the degradation rate measured by C-V hysteresis.

On the other hand, the possibility of integrating high-k(HK) gate dielectrics on Ge substrates has been demonstrated[5], [19]leading to numerous efforts to passivate the interface defects in high-k/Ge MOS structures [19]–[22]. In particular, it has been reported a reduction of D_{it} in (100) Ge MOS capacitors[21] with Post-metal-gate FGA (H_2/N_2) of the atomic layer deposited (ALD)-HfO_2 and ALD-Al_2O_3[10], [21], [23].

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However, despite the extensive literature available about the good interface passivation and excellent device performance obtained with this approach, very few reliability studies of this Ge-based MOS stack have been reported in connection with the interface passivation method by forming gas annealing (FGA). Although NBTI robustness has been shown for SiO_2 passivated Ge-devices[24]–[26], it is clear that more information is needed to describe and model the mechanisms responsible for the degradation of high-k dielectric/Ge stacks.

Among the high-k dielectrics considered for these Ge MOS, HfO_2 emerges as an attractive candidate as it has already proven its quality when paired with Si MOS. Nevertheless,HfO_2 was found to be unstable on GeO_2[27]. On the other hand, Al_2O_3 forms a very good interface with GeO_2[28] but has a relatively low dielectric constant that hardly defines it as a high-k dielectric. A multilayer gate stack (high-k/Al_2O_3/GeO_2/Ge) is then usually propose in the literature, where the high-k is HfO_2. However, a drawback of this multilayer integration is that the addition of materials with a relatively low dielectric constant, lowers the effective dielectric constant of the entire stack. Therefore, HfO_2 has been alloyed with other metal oxides to obtain a ternary metal oxide with improved properties.

In this work, the influence of FGA on the degradation of multi-layered p-Ge/GeO_x/Al_2O_3/HK/MG (MG stands for Metal Gate) stacks, is studied by the dynamics of the flat band voltage (V_{FB}) and C-V hysteresis (V_{hys}) under different polarities of the stressing voltage. Different High-K materials ($HfAlO_x$, $HfGdO_x$ and HfO_2) are considered to analyze the effects of FGA on interface defect passivation, regardless of the HK layer employed.

3. Experimental

The experiments were performed on 300mm p-type *Ge – on – Si* wafers where 1 µm of un-dopped Ge was grown epitaxially on top of the Si substrate. Afterwards, the wafers were cleaned for 30 s in a diluted HF solution (2 wt.%) to remove most of the native oxide. After the HF dip, the Ge surface was re-oxidized in a controlled manner to obtain a GeO_2 layer of ≈ 0.7 nm[28], [29]. Re-oxidation was done during the ALD of ≈ 2 nm Al_2O_3 by means of the *trimethylaluminum* (TMA)/O_3 process. GeO_x (Germanium in oxidation states lower than +4) formation during this ALD process has been described before[30], [31], resulting in a Ge/GeO_x/GeO_2/Al_2O_3 stack. On top of the GeO_x/GeO_2/Al_2O_3 stack, which acts as Interfacial Layer (IL), approximately 4 nm of a Hf-based high-k dielectric was deposited. Such high-k layers consisted of HfO_2, $HfAlO_x$, and $HfGdO_x$ and were all deposited by ALD. The Hf:M atomic ratio is 1:1. The ALD was performed at 300 ◦C in a cross-flow ASM Pulsar 3000 reactor, attached to a Polygon 8300 platform. The precursors used in the ALD process were: $HfCl_4$ and H_2O for HfO_2 deposition and TMA and $Gd(iPrCp)_3$

combined with $HfCl_4$ and H_2O for $HfAlO_x$ and $HfGdO_x$ deposition, respectively. The notation $HfMO_x$ will be used from now on to refer to these Hf-based high-k dielectrics. Pt (40 nm) was used as the gate electrode. Part of the samples underwent a postdeposition forming gas anneal (FGA samples) for 30 min at 400 ◦C in a gas-flow furnace using a forming gas ($90\%N_2+10\%H_2$) ambient, while the rest remained as control samples (no-FGA samples). These annealing conditions were chosen after comparing the results with those obtained with vacuum annealing (10^{-7}Torr, 30 min in 400 ◦C) and they were found to be significantly better. Summarizing, multi-layered stacks under study are approximately 7 nm thick, with a Pt metal gate of 40 nm. Further details about the fabrication process can be found in our previous papers [28], [29], [32].

Capacitance – Voltage (C-V) measurements were carried out using an Agilent 4285A LCR meter. Current-Voltage (I-V) and Constant-Voltage-Stress (CVS) measurements were performed using a Keithley 2636B Source Measurement Unit. During CVS, the stress was periodically interrupted for C-V measurements to track the degradation of the device parameters such as V_{FB} and C-V hysteresis at $V_{FB}(V_{hys})$. For each stress condition, numerous devices (10) were measured. To avoid recovery-related artifacts, we kept constant and small (100 ms) the delay between the C-V measurements and the CVS pulses. The calculation of V_{FB} was performed by the recently introduced inflection point technique[33].

4. Results and analysis

a. Capacitance – Voltage Measurements

Figure 1(a) and (b), show the C-V curves at 200 kHz for both sets of samples, as deposited (no-FGA samples) and with post deposition forming gas annealing (FGA samples). In both cases, the differences between the various Hf based high-k dielectrics in terms of the dielectric constant are noticeable. Considering that the total thickness of the dielectric stack measured by TEM[28] remains the same for all the stacks(≈7 nm),the variation of accumulation capacitance values corresponds to different dielectric constants. The effective dielectric constant for $GeO_2/Al_2O_3/HfMO_x$ multi-layers was found in [28] to be 8.5, 7.7 and 9.5 for $HfMO_x$ being HfO_2, $HfAlO_x$ and $HfGdO_x$, respectively. Note that due to the GeO_2 inter-layer (IL) those values are lower than what it would have been expected for $Al_2O_3/HfMO_x$ bilayers. Moreover, it is observed that the addition of Gd to HfO_2 increases the effective dielectric permittivity, while Al addition decreases it [28]. This conclusion is drawn since the difference between the samples is in the top layer only.

On the other hand, Figures 1(c) and (d) present the multi-frequency (200Hz - 300 K Hz) C-V curves measured at room temperature for the no-FGA and FGA HfO_2 samples, respectively. A larger frequency

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dispersion is observed for the no-FGA HfO_2 (Figure 1(c)) from depletion into accumulation with respect to its FGA counterpart (Figure 1(d)) in the same biasing region. This indicates that FGA leads to the effective passivation of defects with energies lying near the Ge valence band (VB)[21]. The $HfGdO_x$ and $HfAlO_x$ samples are not plotted in the figure because they have similar behavior. With regard to the dispersive features (also known as the "weak inversion hump") observed in the depletion to inversion region (gate biases greater than V_{FB}) they are caused by trapping and detrapping of electrons and/or holes at traps with energies between approximately mid-gap and the Ge conduction band (CB), located close to the interface [21].

Given that the area under this "weak inversion hump" and the C-V stretch-out are proportional to the amount of mid-gap states[28], we observed a reduction of these states in all $HfMO_x$ samples after the FGA treatment. This is well in agreement with previous results presented by Fadida et al [28] for a set of samples with a very similar composition and also agrees with previous reports that indicate that post-metal-gate FGA (H_2/N_2) of ALD-HfO_2 and ALD-Al_2O_3 dielectrics significantly reduces the interface state density[21], [34], [35]. The D_{it} for both FGA and no-FGA stacks, have been calculated around mid-gap using the High-Frequency – Low-Frequency (Castagné-Vapaille) and conductance methods[36]–[38]. The inset of Figure 1(a), shows the D_{it} profile around mid-gap for the case of HfO_2 as the high-K dielectric as function of the surface potential Ψ_S, calculated according to the Berglund's Integral[36] for the HF-LF method, and by the trap response time estimated with the Shockley–Read–Hall statistics of capture and emission rates for the conductance method[38]. It reveals that for both the HF-LF and conductance methods, the no-FGA samples are the most defective. As well as it happens with the Multi-Frequency C-V curves, D_{it} for the $HfGdO_x$ and $HfAlO_x$ samples are not plotted in the figure because they have a very similar behavior to the HfO_2 samples.

It should be pointed out that, for both extraction methods, no clear differences can be observed between the stacks with different HK oxides deposited on top of the IL. This observation points towards the fact that in our samples, the IL ($GeO_x/GeO_2/Al_2O_3$ stack of ≈3nm measured in [28]) effectively screens the effects of HK defects on the quality of the MOS stack in terms of D_{it}[39], [40], due to its 3nm thickness. In this scenario, the discussion is centered on the effects of FGA on the degradation characteristics of the samples under voltage stress, and not on the influence of the HK layer.

Finally, it is worth noting that although both the Castagné-Vapaille (HF-LF)[37] and conductance[36] methods at room temperature (RT) vary in their accuracy when they are used to evaluate D_{it} near the band gap edges for low band-gap semiconductors, they have been widely used in the literature

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to evaluate D_{it} around mid-gap[28], [41]–[45]. In this study, both techniques were employed to make a relative comparison of the D_{it} at mid-gap [28], [38], [41] before and after the FGA. Moreover, the results obtained are consistent with recent reports [21], [24], [38], [41].

b. Electrical stress measurements

To clarify the role of the post deposition forming gas annealing (FGA) in the electrical stress measurements, the degradation characteristics of $Al_2O_3/HfMO_x$ multi-layers under constant voltage stress (CVS) are studied in terms of the relative shift in V_{FB} (ΔV_{FB}) as function of the stress voltage pulse of short duration (≈1 s), at positive and negative bias. For negative bias, V_{FB} was measured from consecutive C-V curves at 200 kHz while decreasing in each C-V hysteresis loop the minimal DC bias point in accumulation (namely, the stress voltage in Figure 2(a), V_{stress}), but keeping the same maximal DC bias point in inversion (namely, the start voltage in Figure 2(a), V_{start}). The resulting C-V plots for the HfO_2 samples can be observed in Figures 2(a) to 2(d) (FGA and no-FGA, positive and negative bias stress) and the measurement methodology is depicted in Figure 2(e). ΔV_{FB} was calculated as $\Delta V_{FBN} = V_{FBN} - V_{FB0}$, with V_{FBN} being the flat band voltage extracted from the n^{th} CV-curve in the inversion to accumulation sweep, and V_{FB0} the flat band voltage extracted from the first inversion to accumulation sweep. Then, a positive ΔV_{FB} represents a shift in V_{FB} towards positive bias, while a negative ΔV_{FB} the opposite. Since the recovery of trapped charge for the $Al_2O_3/HfMO_x$ bilayered MOS system can be fast[24], [46], special attention was paid to keep the delay between measurements constant and small (100 ms). This methodology, extensively used to stress MOS stacks[18], [25], [46], [47], allows short delay times between voltage steps, maximizing the speed of the sweep for the available instruments, thus reducing the percentage of trapped charge removed during the delay time and avoiding recovery-related artifacts[25],[46].

Figure 3(a) shows the effect of V_{stress} on the shift of V_{FB} for all the sets. V_{FB} shift towards negative bias (negative ΔV_{FB}) indicates hole trapping. Among annealed samples (i.e. FGA samples), a similar shift of V_{FB} is observed as function of the stress voltage (V_{stress}), which is clearly smaller than the shift in the no-FGA samples. Similarly, Figure 3(b) shows the evolution of ΔV_{FB} measured from consecutive C-V curves at 200 kHz while increasing the maximal DC bias point in inversion (namely, the start voltage in Figure 3(b), V_{start}), and keeping the same minimal DC bias point in accumulation (V_{stress}) (see Figures 2(b) and (d)). Contrary to the previous case, V_{FB} shift towards positive bias (positive ΔV_{FB}) indicates accumulation of negative charge. Moreover, the no-FGA and FGA samples show the same trend.

On the other hand, Figure 3(c) and (d) show the relative variation of the C-V hysteresis voltage measured at V_{FB} from C-V curves in retrace mode, sweeping the gate bias from inversion to accumulation

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and back to inversion (C-V hysteresis loop) using the same methodology as for the measurements of V_{FB}. ΔV_{Hys} was calculated as $\Delta V_{Hys} = V_{HysN} - V_{Hys0}$, with V_{HysN} being the Hysteresis voltage extracted from the n^{th} CV-curve hysteresis loop, and V_{Hys0} the hysteresis voltage extracted from the first hysteresis loop. Then, a positive ΔV_{Hys} represents an increase in the hysteresis width. Figure 3(c) shows the effect of the minimum bias in accumulation (V_{stress}) on the width of the C-V hysteresis, while keeping the same starting DC bias point in inversion (V_{start}). It is observed that the no-FGA samples show higher ΔV_{hys} as V_{stress} increases, although such difference is not as large as in the case of ΔV_{FB} (Figure 3(a)). However, if ΔV_{hys} is measured in consecutive C-V curves while increasing the maximal DC bias point in inversion (V_{start}), with the same minimal DC bias point in accumulation (V_{stress}), the ΔV_{hys} increases without significant variations between no-FGA and FGA samples. Therefore, the main difference between FGA and no-FGA samples arises for the case of the negative stress. To exclude any hot carrier injection mechanism to be responsible for such variations, Current-Voltage curves of the samples are shown in Figure 4(a) and (b), for no-FGA and FGA samples, respectively. It can be seen that for the voltage range (0 to -4V approx.) applied to the stacks during the stress, the current through it does not surpass the 1nA limit.

c. Stress as function of time

In order to assess the influence of the stressing time and confirm the results obtained under stress at negative bias in Figure 3(a), the evolution of the flat-band voltage was studied as function of the stress time at a constant voltage. This was done by applying a constant $V_G - V_{FB}$ voltage, while measuring the C-V hysteresis curve in the retrace mode (where the voltage was swept from inversion to accumulation and then back to inversion) at regular intervals[18]. Following a similar procedure, C-V hysteresis curves were also measured during a recovery process at room temperature (RT) without biasing the stack, which followed the previously mentioned CVS. The results obtained are presented in Figure 5(a) and (b), and it is interesting to note that V_{FB} shift is always more significant in the case of the non-annealed samples (no-FGA samples). Furthermore, the shift towards negative bias of the flat-band voltage suggests the accumulation of positive charge in the gate oxide confirming the results of Figure 3. Measurements of the V_{FB} shift (Figure 5 (a)) here presented have been fitted by an exponential law $\Delta V_{FB} = Ae^{(-\frac{t}{\tau})}$ in both the stressing and recovery periods (fits not shown), revealing time constants of around 20 to 100 seconds in the stressing period (from 0 to 750 sec. approx.), and 200 to 600 seconds in the recovery part (from 750 to 150 sec. approx.). In this manner, not only is the recovery process incomplete, but also slower than the degradation process (it takes longer for the samples to partially recover).

It should be noted that the current level for the bias used in Figure 5 ($V_G - V_{FB}$= -3.5V) is in the order of 100pA for both sets of samples (see I-V measurements shown in Figure 4)to avoid charge build-up due to higher leakage currents.

Moreover, we also observe recovery of the flat band voltage during the RT relaxation without biasing the stack. Although the recovery of V_{FB} after CVS is not the scope of this work, the magnitude of this effect is consistent with earlier reports[18]. The characteristic time during the annealing phase is very long, as it takes some minutes for the partial recovery of V_{FB}. Therefore, it is clear from this observation that the small values of delay (100ms) between measurements will not affect the main observation of our work: flat band voltage shift is larger in the case of the no-FGA samples when compared to the FGA ones, for the same stressing conditions at negative bias (Figure 3 (a) and (c), and Figure5).

It's worth noting that the degradation dynamics of stacks with different HK oxides show differences that are well in agreement with the literature: for HfO_2, the C-V hysteresis is wider and it is strongly reduced after FGA process, while though for ternary oxides the reduction is still observed, the effects are not as pronounced[48]. The origin of such differences, possibly related to deep trapping and bulk oxide defects, is not on the scope of this work.

5. Discussion

By comparing the dynamics of V_{FB} and the C-V hysteresis, relevant observations can be made regarding the role of the post deposition FGA in the degradation characteristics under voltage stress. At negative bias, Figure 3(a) and (c), the V_{FB} and V_{hys} as function of V_{stress}-V_{FB} show different behavior between both set of samples (FGA and no-FGA samples). In the FGA samples, the V_{hys} shows a monotonous increase up to +0.4 V in the bias range from -1.5V to -3.5V, while V_{FB} does not show relevant variations (<0.1V) in the same bias range. This is coherent with the fact that the repeated C-V hysteresis sweeps overlap the 1st C-V hysteresis in the upward sweep direction (Figure 2(c)), when the MOS capacitor is measured from inversion to accumulation (small V_{FB} variations), indicating that the majority of charge trapping is a reversible process. On the contrary, no-FGA samples show a much steeper decrease of V_{FB} while the C-V hysteresis also increases, indicating that the positive charge trapping is permanent. This difference in the level of hole trapping is also observed in Figure 5(a) and (b), where the no-FGA samples clearly exhibit a higher level of hole trapping.

The permanent characteristic of the charge trapping observed in the no-FGA samples, may be related to a higher barrier for the trapped holes to be removed from the traps[32]. On the other hand,

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The higher level of positive charge trapping in the no-FGA samples compared to their FGA counterparts may be related to a higher density of hole traps with energy levels aligned with the semiconductor valance band edge (i.e. negative bias on the gate contact on Ge-p substrate). In a recent paper, Zhang et al[21] reported direct experimental evidence using Soft and Hard X-rays synchrotron photoelectron spectroscopy about the chemical states of germanium in the Ge/ALD-Al_2O_3 region during FGA. It shows that the Germanium oxide (GeO_x, Germanium in oxidation states lower than +4) formed at the high-K/semiconductor interface can significantly degrade the electrical quality of the entire structure by introducing traps at energy levels near the Conduction Band (CB) (namely, electron traps) and Valence Band (VB) (namely, hole traps). Nevertheless, it is also shown that such traps are selectively passivated during the forming gas annealing.

In this regard, the experimental evidence in Ref. [21] leads to a model which proposes that, during FGA, hydrogen (present in the forming gas atmosphere) may diffuse to the Al_2O_3/Ge interface and react with residual hydroxyls incorporated during the growth of the ALD-Al_2O_3, producing H_2O. The water molecules thus formed can further react with Ge and GeO_x to form GeO_2 (a less defective Ge oxide) reducing the density of defects at the interface. It is worth to mention that this proposed reaction is consistent with prior experiments on high-k oxides on Ge substrates[10], [23], and that the existence of GeO_x in HF cleaned substrates prior FGA, has been widely documented in the literature[30], [49], [50]. Also, the Pt gate helps to dissociate H_2 to atomic H, which may contribute to the reaction with the -OH group in the ALD-Al_2O_3 and, therefore, to GeO_2 formation.

Additionally, the interface bonding configuration between Ge and an overlying suboxide or oxide layer, has been also studied by first-principles modeling by Zhang et al in [21]. The results show that Ge/GeO_2 has a defect free interface within the Ge band gap, while the Ge/GeO_x/GeO_2 structure can have a large density of defect states (O deficiency defects) with energy levels near the CB (electron traps) and VB (hole traps) edges, which agrees well with the existing literature[34], [35]. Furthermore, hydrogen also reacts with these defects, removing both the electron and hole traps from the band gap energy range[21].

For positive bias stress, shown in Figure 3(b) and (d), where the V_{FB} and V_{hys} are studied as function of V_{start}, both parameters show a monotonous increase without differences between FGA and no-FGA samples, indicating accumulation of negative charge. This may suggest that the electron trapping (V_{FB} shift towards positive bias) happening for the positive stress is being caused by traps generated during the voltage stress. This interpretation is supported by the increase in ΔD_{it} around mid-gap (this is, the increase of D_{it} with respect to the D_{it} around mid-gap for the fresh samples) estimated for the sample being stressed during each single frequency capacitance voltage loop measurement performed during the CVS stress,

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and the results are summarized in the inset of Figure 2(d). It shows that for positive stress the increase in D_{it} is larger than for the negative stress, indicating that when charge is injected from the substrate, the damage in the interface results more significant.

As previously mentioned, H present in the FGA atmosphere reacts with the defects at the $Ge/GeO_x/GeO_2$ interface removing both the electron and hole traps from the band gap energy range. However, the energy barrier for removing those different trap states (holes and electrons) is not the same, being larger the energy required for electron traps passivation [21], [51]. Thus, the reduced impact of the FGA on the passivation of electron trap states, may also contribute to the lack of differences between FGA and no-FGA samples stressed at positive bias.

Summarizing the overall results, it is observed that the stress at negative and positive bias contribute with hole and electron trapping respectively, based on the shift of the V_{FB}. The main feature occurs at negative bias, where strong dependence on the FGA process is observed. It is worth mentioning that there is a common trend regardless of the $HfMO_x$ stack deposited on top of the $GeO_x/GeO_2/Al_2O_3$ IL growth on top of the Ge substrate. This indicates that the $GeO_x/GeO_2/Al_2O_3$ IL may play a determinant role in the dependence on the FGA process. Nevertheless, the thickness of the $GeO_x/GeO_2/Al_2O_3$, around 3 nm, may be too large for the $HfMO_x$ layer to influence the charge trapping phenomena[39], [40], which is usually assumed to happen in the vicinity of the interface. Further investigation with thinner ILs should be made in order to clarify the impact of these various HK materials.

6. Conclusions

The influence of forming gas annealing on the degradation under voltage stress of multi-layered germanium-based Metal-Oxide-Semiconductor capacitors ($p\text{-}Ge/GeO_x/Al_2O_3$/High-K/Metal Gate) has been analyzed in terms of the C-V hysteresis and flat band voltage shift as function of both negative and positive stress fields.

Regardless of the stress field and duration of the stress pulse, it is observed that the stress at negative and positive bias contributes with hole and electron trapping respectively. The main feature occurs under negative bias stress, where strong dependence on the FGA process is observed.

The possible reasons for a higher level of positive charge trapping in the no-FGA samples compared to the FGA samples at negative stress fields is related to a higher density of hole traps with energy levels aligned with the semiconductor valance band edge. The FGA produces a selective passivation of traps at

the interfacial layer with energy levels near the Conduction Band (electron traps) and Valence Band (hole traps) edges, with the energy barrier being smaller for the passivation of the latter.

Finally, it is worth mentioning the challenges arising from this behavior when addressing the hybrid integration of Ge technologies with III-V substrates. For the latter, surface treatment is almost mandatory in order to achieve a reduced D_{it} profile, however it contributes to the charge generation in the dielectric stack, mainly because of the de-passivation of the traps at the dielectric / semiconductor interface. This implies that the improvement of the high-K/InGaAs interface does not necessarily mean an increase of the reliability of the MOS stack. On the contrary, Ge-based MOS stacks show a different behavior, where FGA reduces both the D_{it} and the charge trapping in Ge stacks, affecting the shift of the flat band voltage. Therefore, summarizing the experimental results presented in this paper regarding Ge based MOS stacks, and taking into account previous literature about the degradation mechanisms in InGaAs –based MOS stacks, we find that a final post metallization forming gas (H_2/N_2) annealing step may affect the degradation rate of Ge and InGaAs based MOS stacks in a different way. While charge trapping is reduced in HK/GeO_2/Ge stacks after FGA, the opposite is observed in HK/InGaAs stacks. Proper FGA conditions to improve the HK/semiconductor interface without affecting the stack's reliability are therefore a key to unleash the development of hybrid technologies.

The results presented in this paper contribute to a better understanding of the limiting factors of Ge and III-V (InGaAs) channel devices on a silicon substrate, paving the way for a high performance low power CMOS technology of high mobility channel materials on Si.

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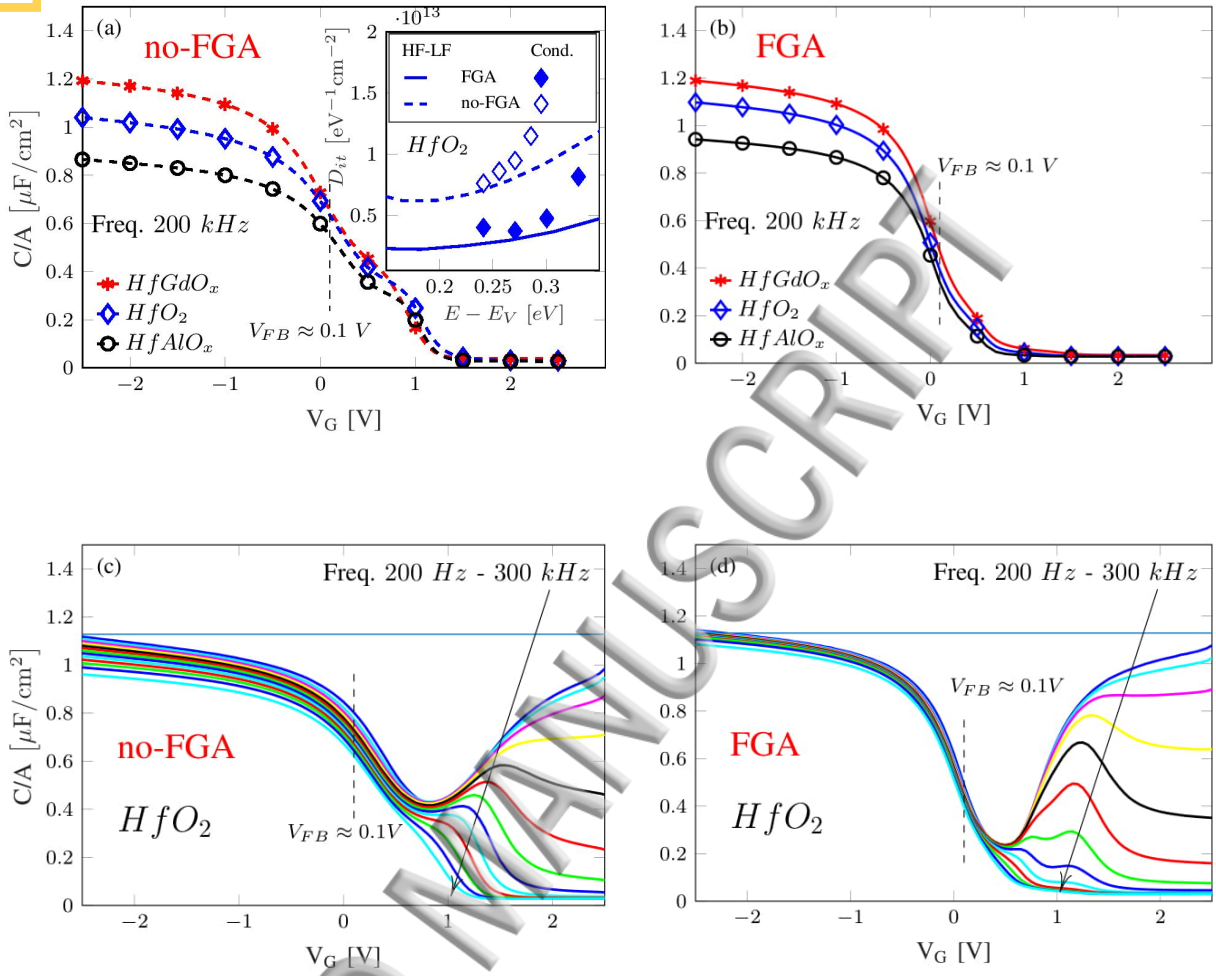

Figure 1. Capacitance - Voltage curves for the samples being studied measured at 200 kHz. (a) Samples without forming gas annealing, and (b) samples with forming gas annealing. In each plot the arrow points out the flat band voltage, calculated according to the inflection point technique. The inset in (a) shows the D_{it} for the HfO_2 samples calculated using the HF-LF method (dashed blueline corresponds to no-FGA and solid blue line to FGA samples) against the conductance method (filled and solid diamond markers, for no-FGA and FGA, respectively). In both cases, D_{it} are higher for the no-FGA sample. Subfigures (c) y (d) shows de Multi-Frequency capacitance-voltage measurements (200 Hz – 300 kHz) for HfO_2 stacks, pre and post the FGA step, respectively. A reduction in the frequency dispersion in accumulation in the FGA sample is clear as well as a higher weak inversion hump, which is consistent with the reduction in D_{it}.

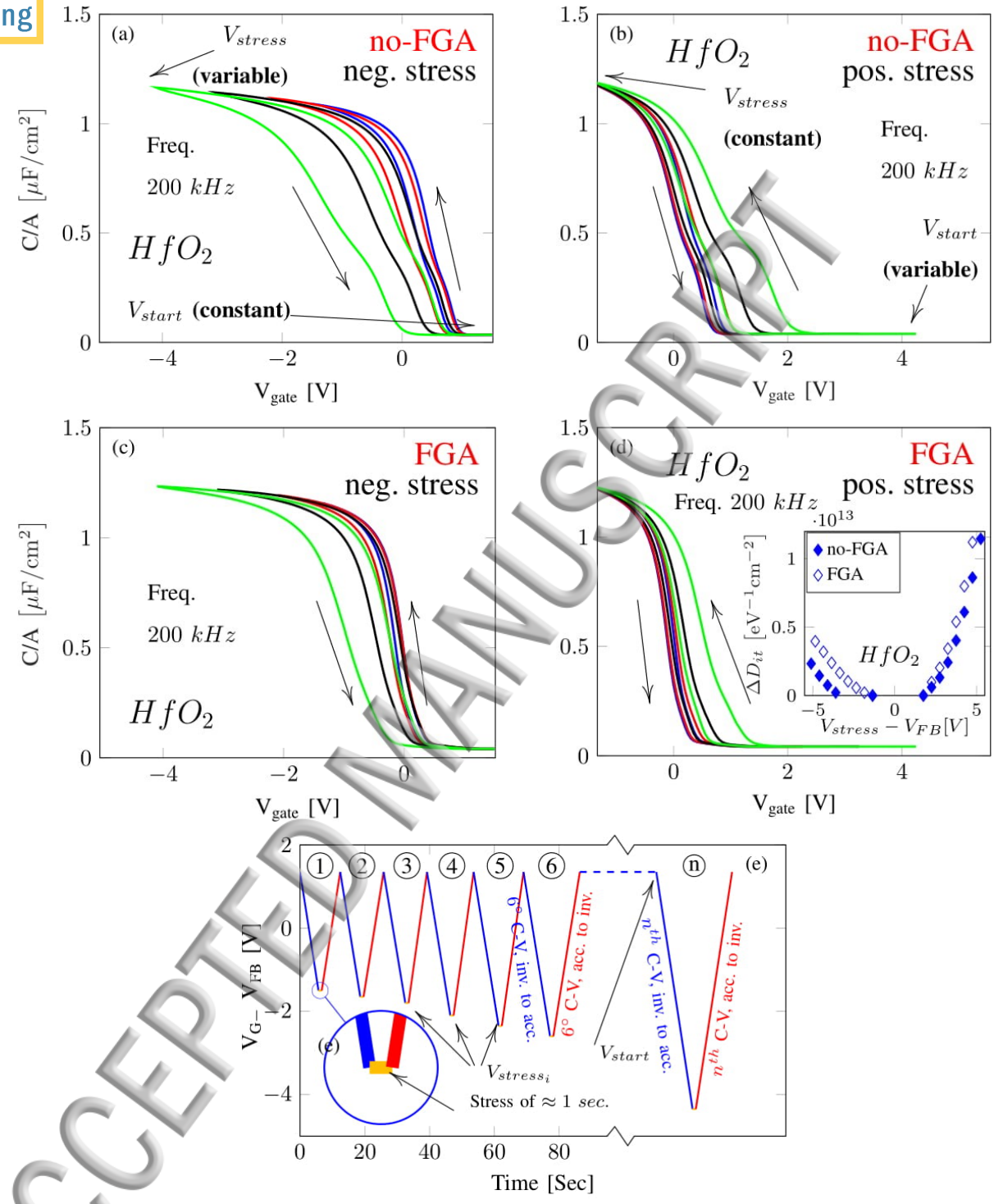

Figure 2. Single Frequency Capacitance – Voltage hysteresis measurements. Without Forming Gas Annealing (no-FGA) samples negatively (a) and positively (b) stressed. Forming Gas Annealing (FGA) samples are shown in (c) and (d) for negative and positive stress voltages. The inset of (d) shows the evolution of D_{it} as function of V_{stress} and V_{start} respect to the fresh sample (ΔD_{it}) for each stress calculated at mid-gap. The evolution of the stressing voltage is shown in (e) for the case of the negative voltage stress, along the consecutive C-V loops. V_{stress} and V_{start} are also pointed in figures (a) and (b) for the negative and positive voltage stress, respectively.

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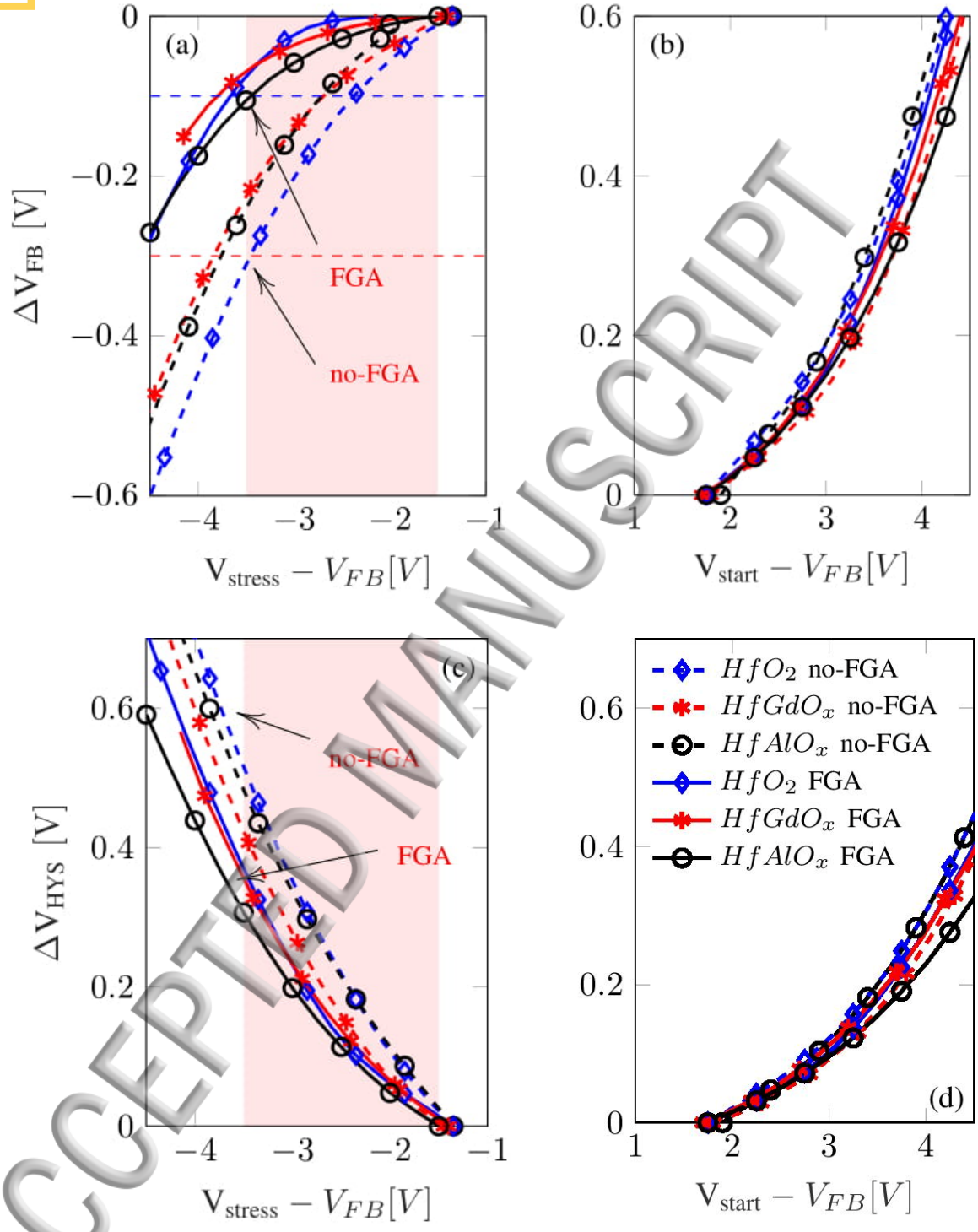


Figure 3. ΔV_{FB} and ΔV_{Hys} for the different multi-layered samples for negative and positive voltage stress (decreasing V_{stress} and increasing V_{start}, respectively). Samples without FGA stressed with negative (a) and positive (b) bias. Samples without FGA with negative (c) and positive (d) bias. Red and blue dashed lines indicate in (a) the maximal variation of the V_{FB} in the range of -3.5 V to -1.5V (shadowed zone) for no-FGA and FGA, respectively.

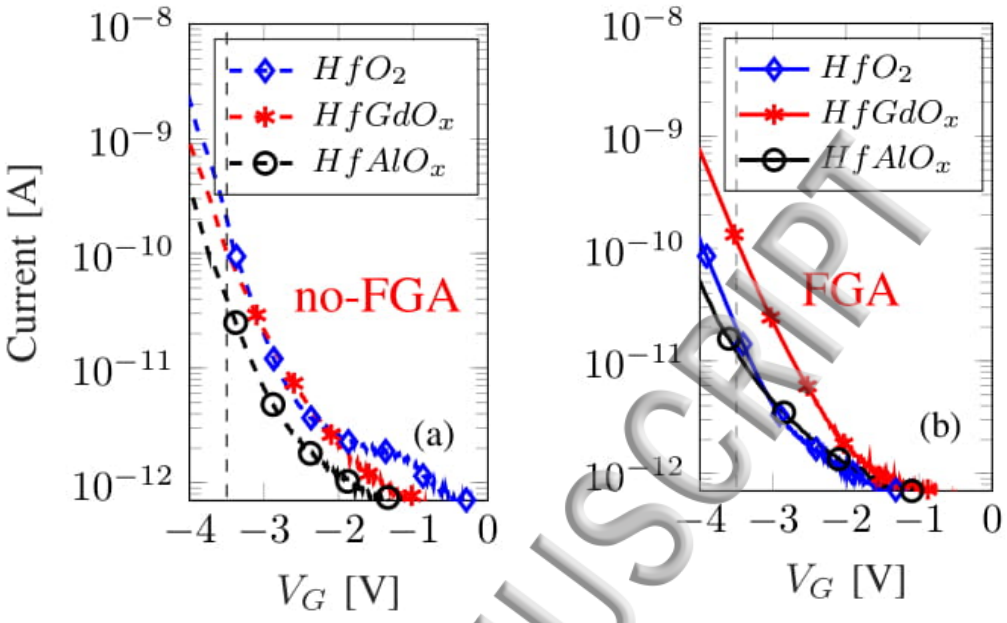


Figure 4. Voltage-Current measurements. (a) no-FGA samples, (b) FGA samples. Current results slightly higher for no-FGA samples.

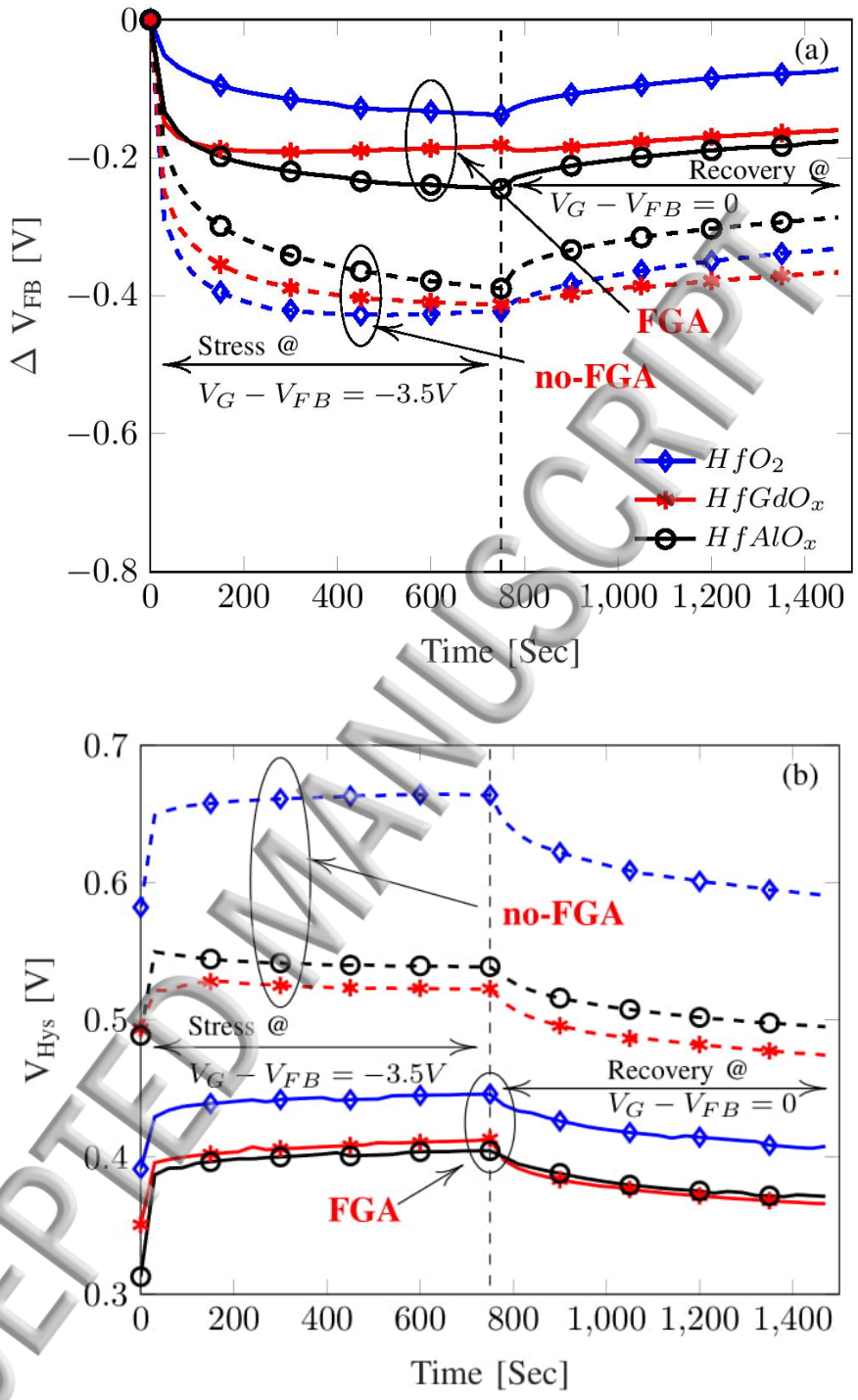
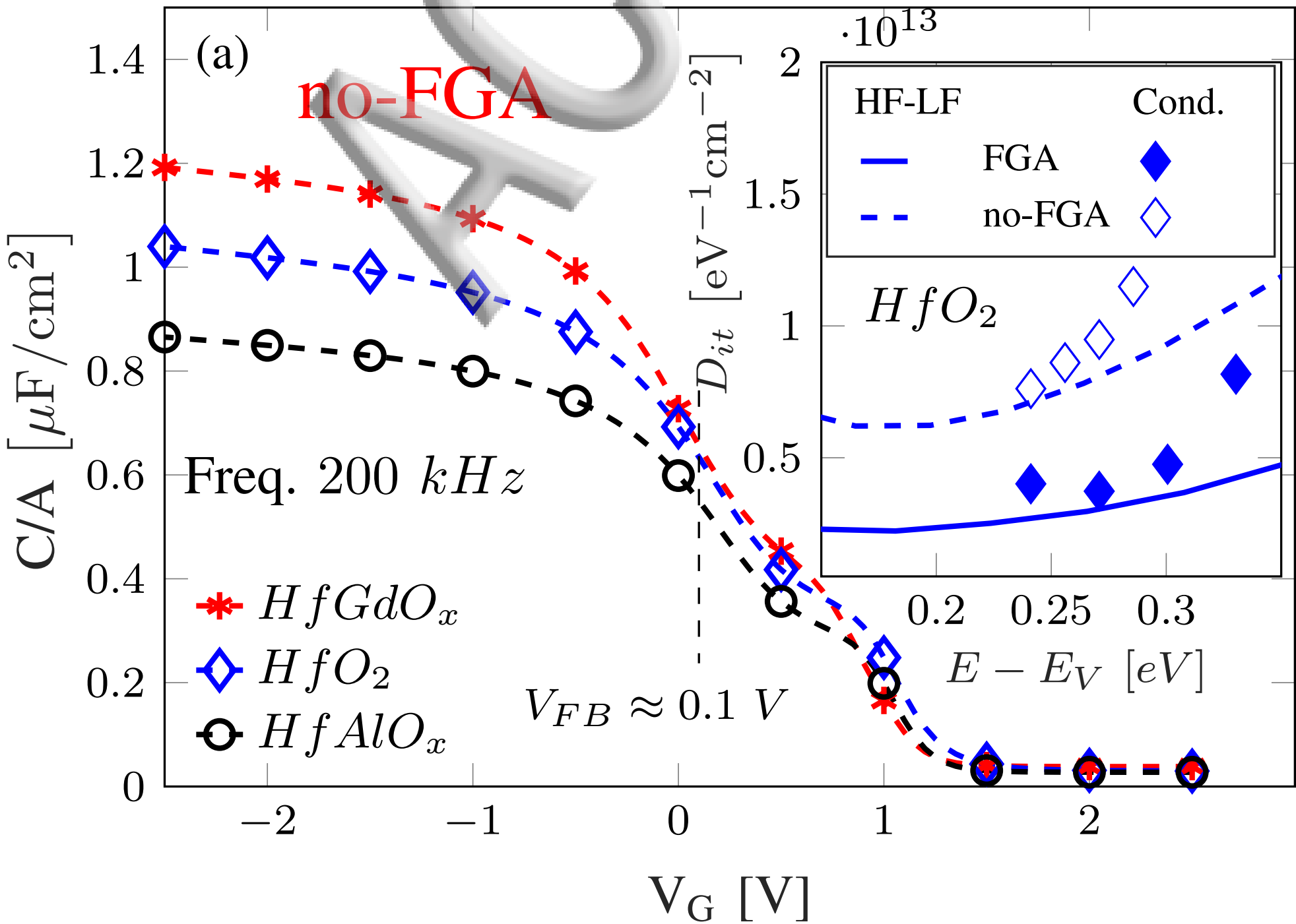
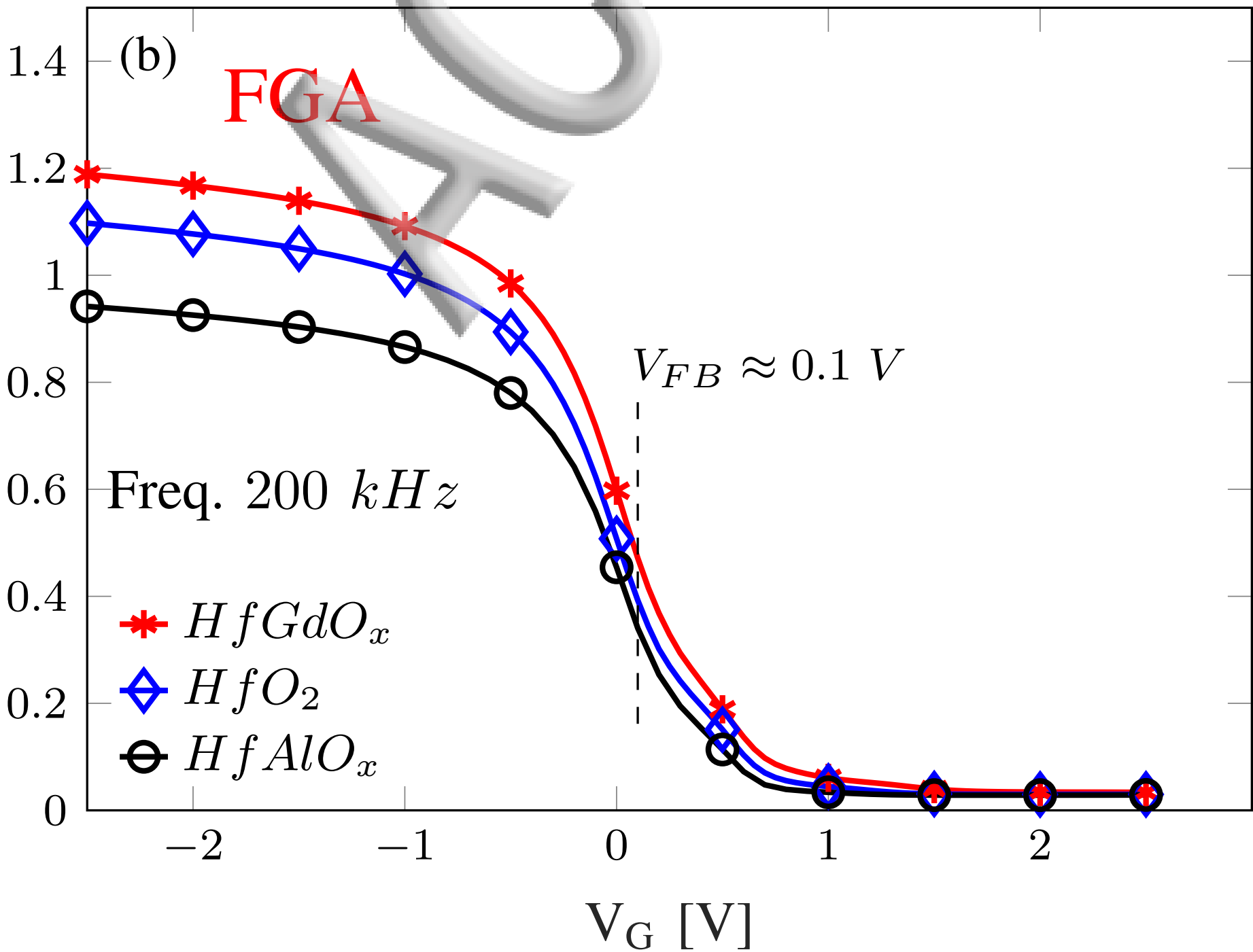
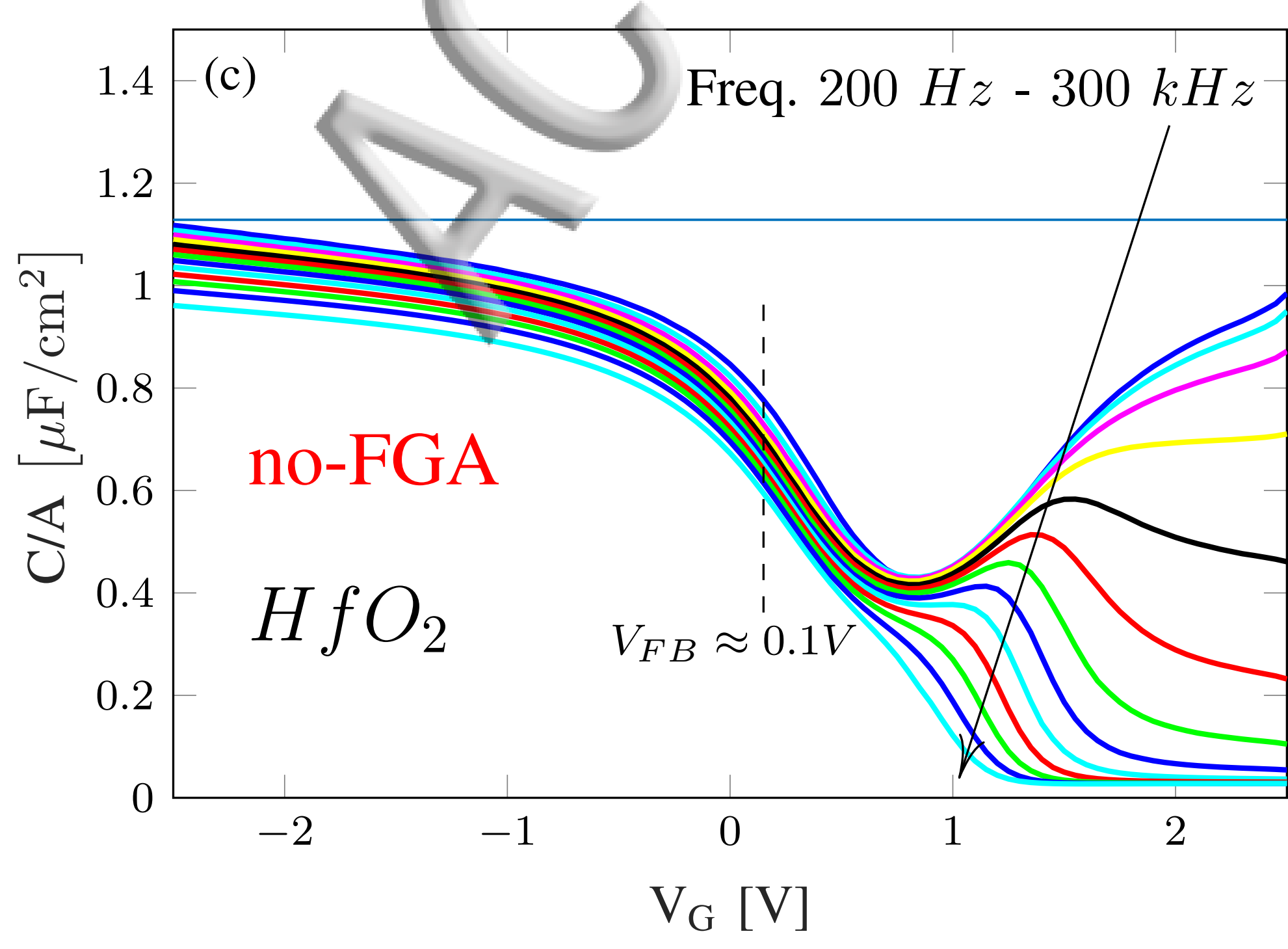
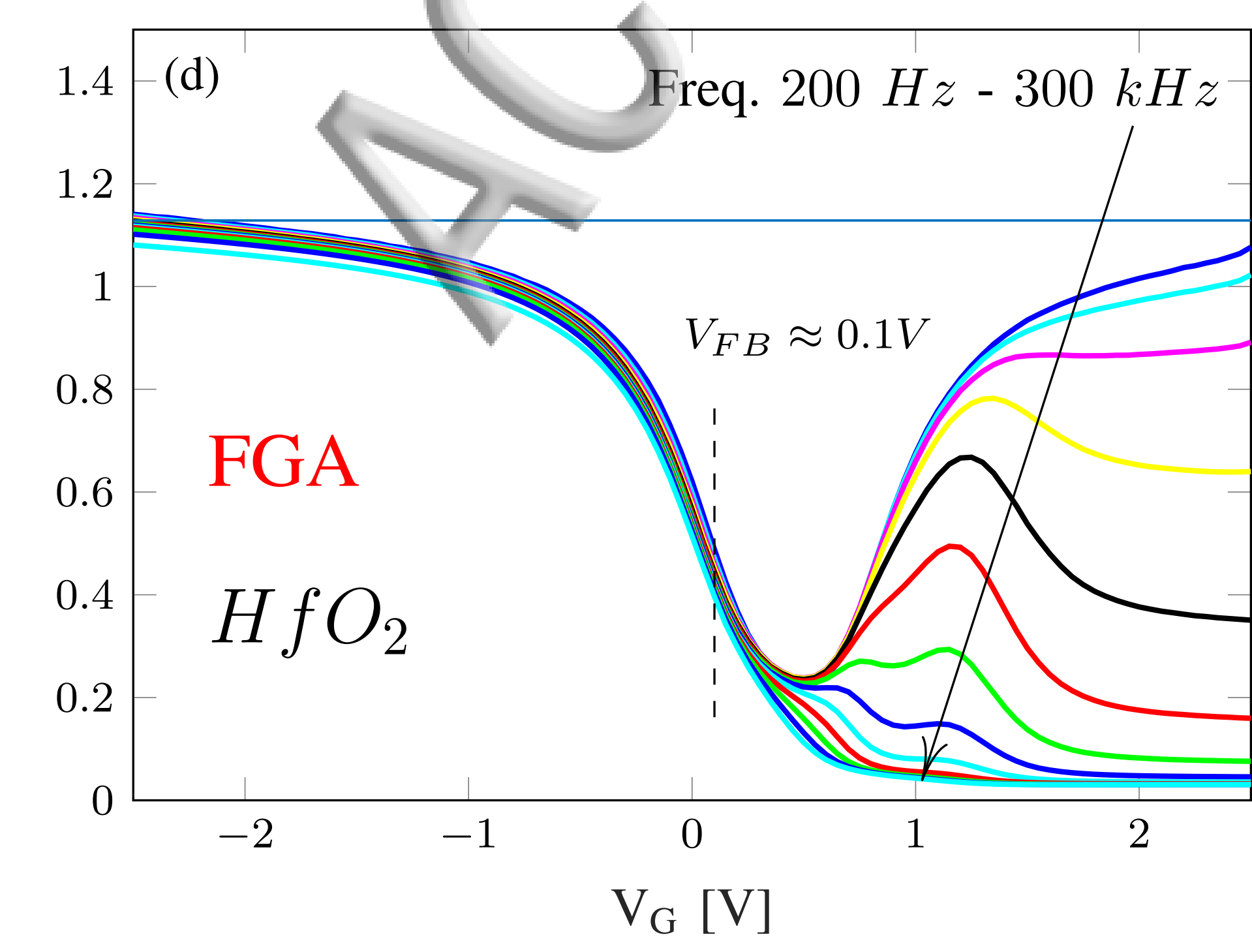


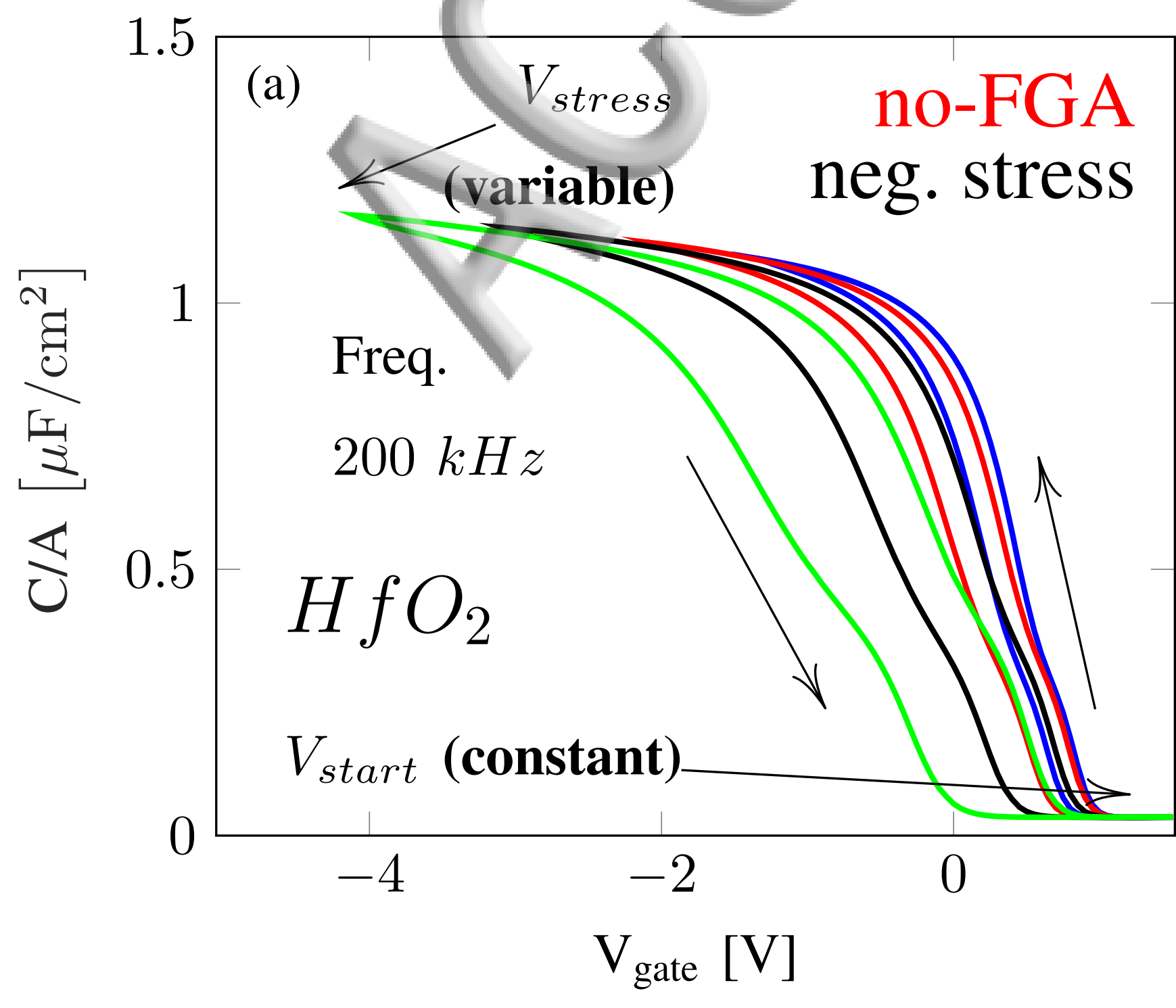
Figure 5. Impact of FGA on the V_{FB} shift (a) and C-V hysteresis (b) of the different stacks for longer stressing times (30 sec.). It can be seen how the FGA reduces both the ΔV_{FB} and the V_{hys} in all sets of samples.

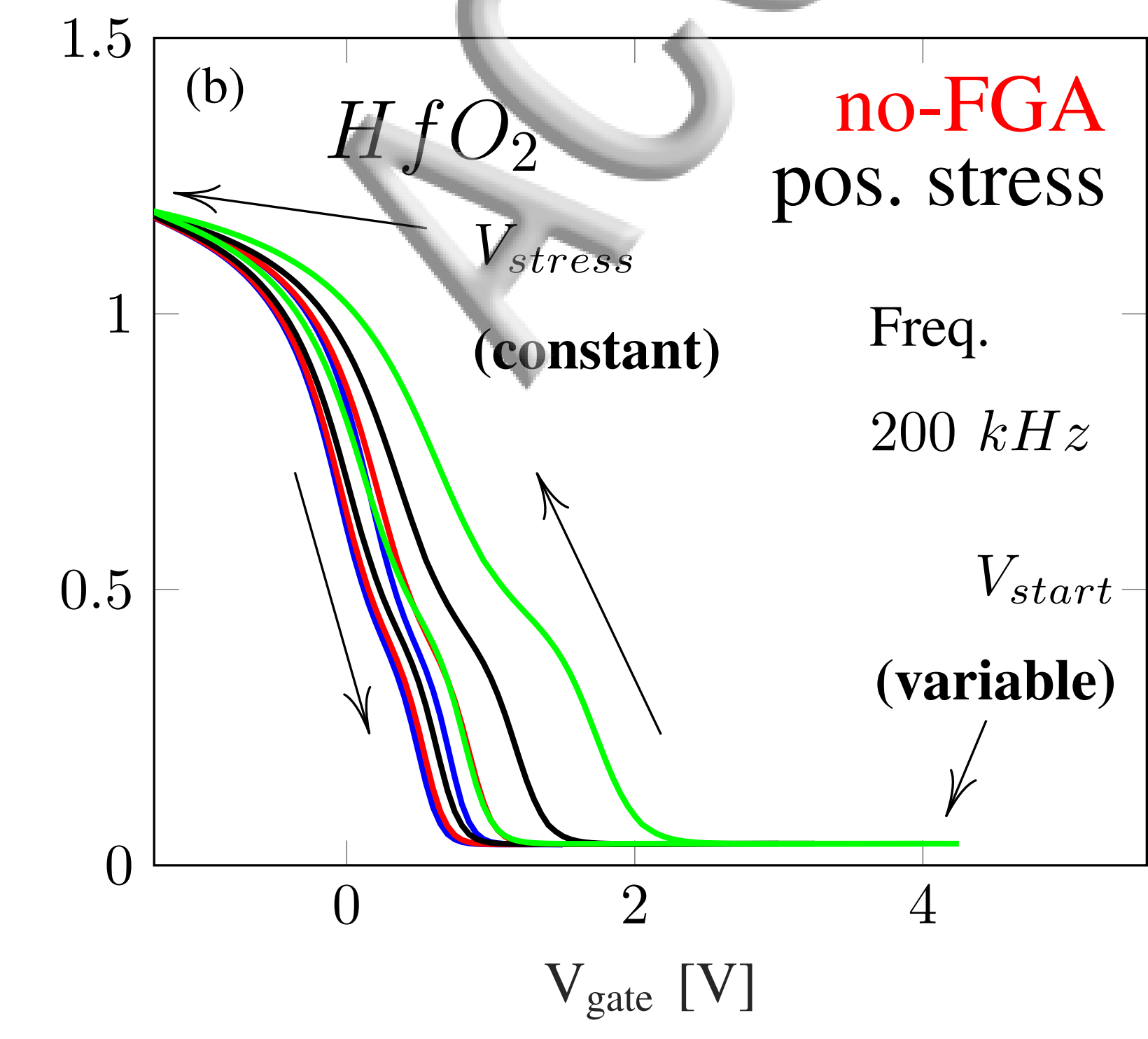

(a)
no-FGA
Freq. 200 kHz
$HfGdO_x$
HfO_2
$HfAlO_x$
$V_{FB} \approx 0.1\ V$
C/A $[\mu F/cm^2]$
V_G [V]
D_{it} $[eV^{-1}cm^{-2}]$
$\cdot 10^{13}$
HF-LF
Cond.
FGA
no-FGA
HfO_2
$E - E_V$ $[eV]$

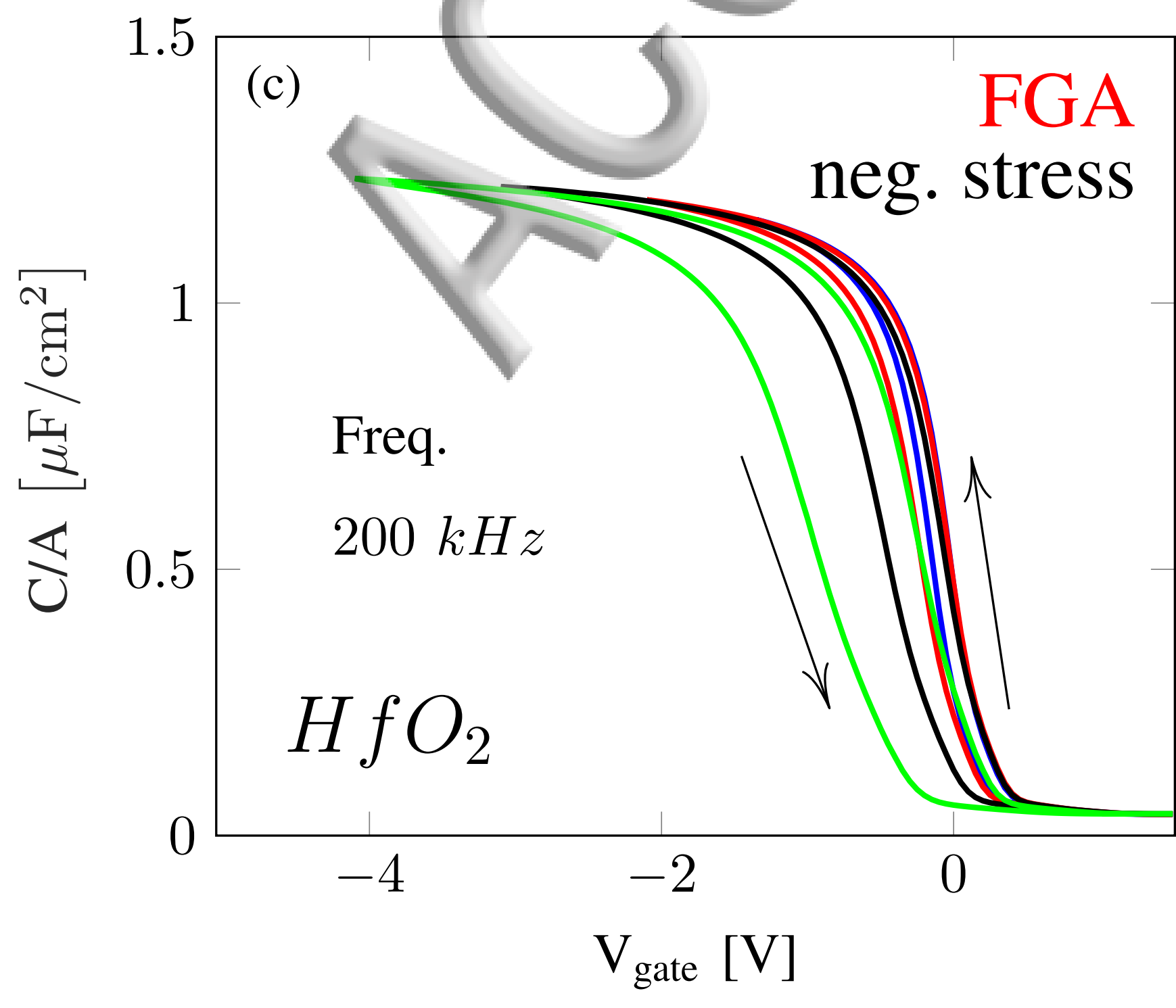

(b)
FGA
$V_{FB} \approx 0.1\ V$
Freq. 200 kHz
$HfGdO_x$
HfO_2
$HfAlO_x$
1.4
1.2
1
0.8
0.6
0.4
0.2
0
−2
−1
0
1
2
V_G [V]

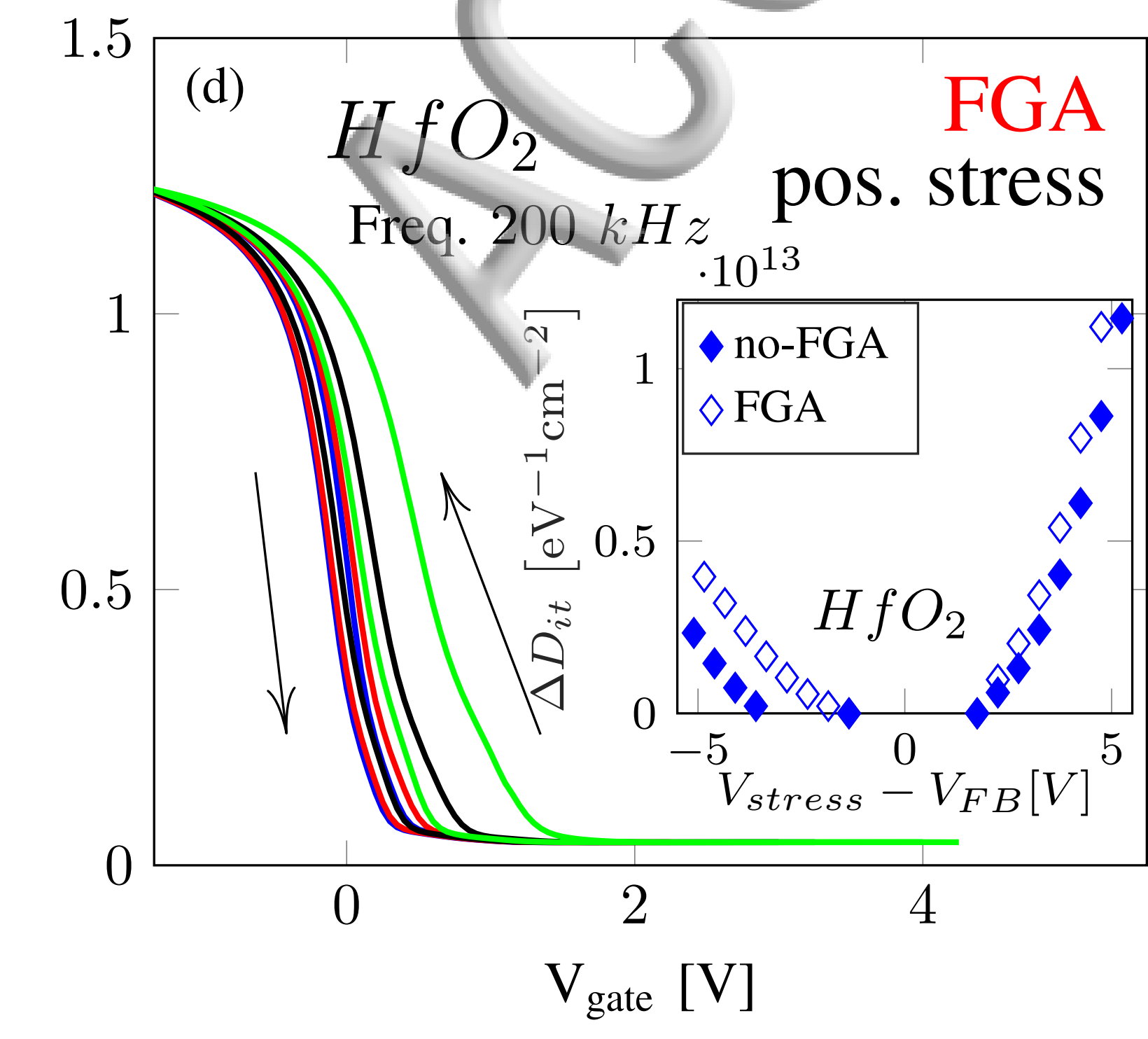

(c)
Freq. 200 Hz - 300 kHz
no-FGA
HfO_2
$V_{FB} \approx 0.1V$
C/A $[\mu F/cm^2]$
V_G [V]
1.4
1.2
1
0.8
0.6
0.4
0.2
0
−2
−1
0
1
2

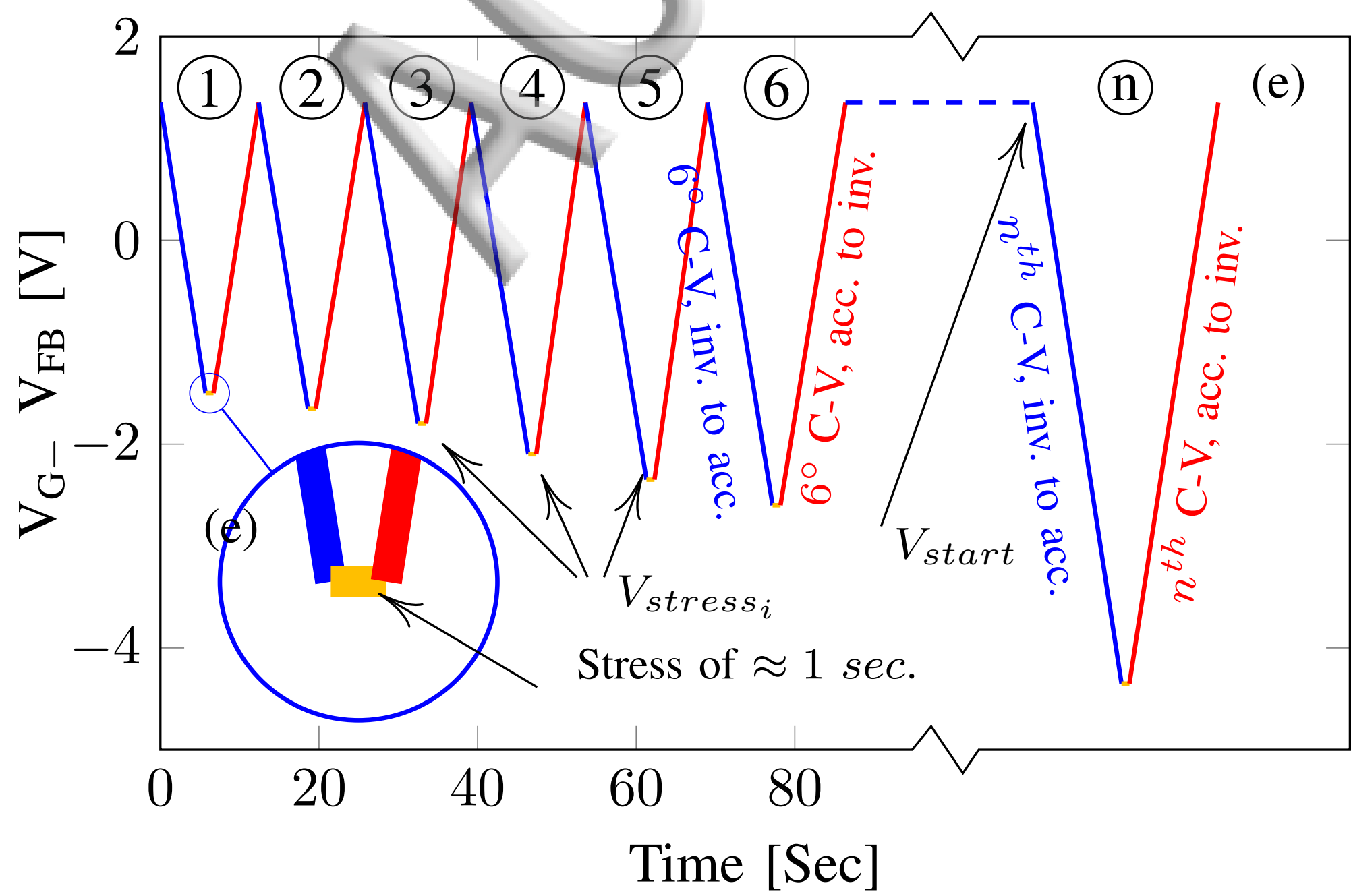

(d)
Freq. 200 Hz - 300 kHz
$V_{FB} \approx 0.1V$
FGA
HfO_2
1.4
1.2
1
0.8
0.6
0.4
0.2
0
−2
−1
0
1
2
V_G [V]

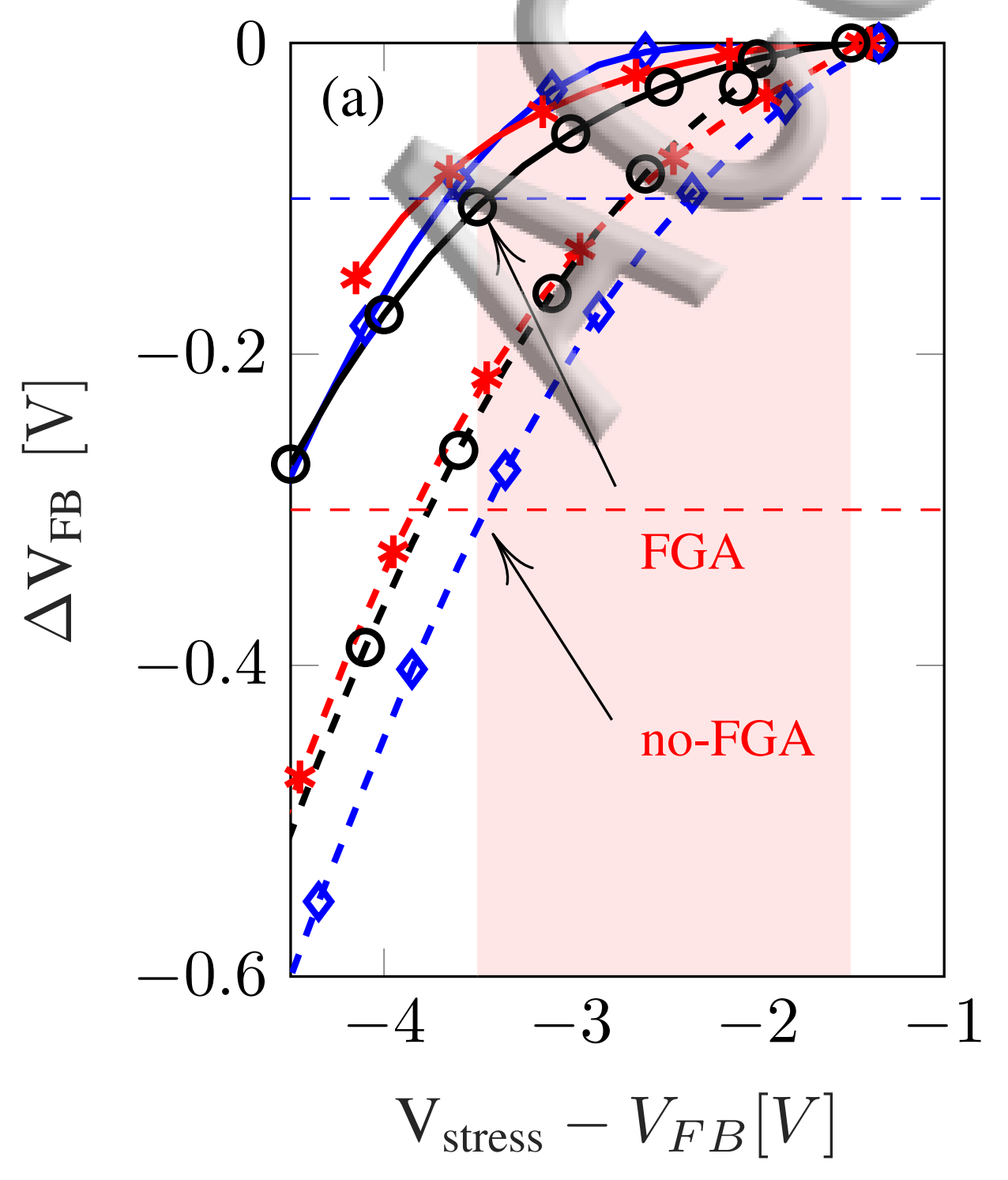

(a)
V_{stress}
(variable)
no-FGA
neg. stress
Freq.
200 kHz
HfO_2
V_{start} (constant)
C/A [μF/cm^2]
1.5
1
0.5
0
−4
−2
0
V$_{gate}$ [V]

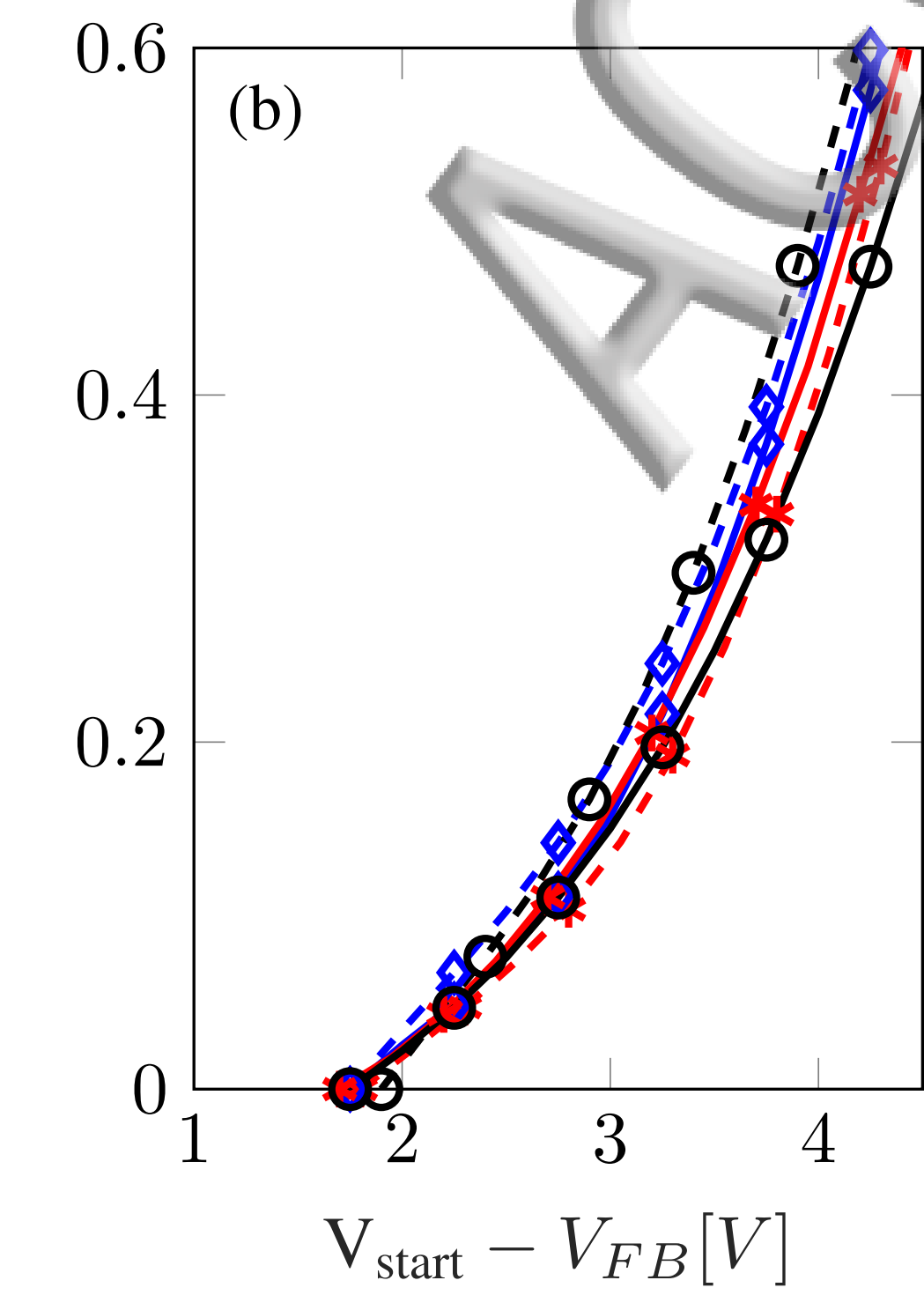

(b)
HfO_2
no-FGA
pos. stress
V_{stress}
(constant)
Freq.
200 kHz
V_{start}
(variable)
1.5
1
0.5
0
0
2
4
V_{gate} [V]

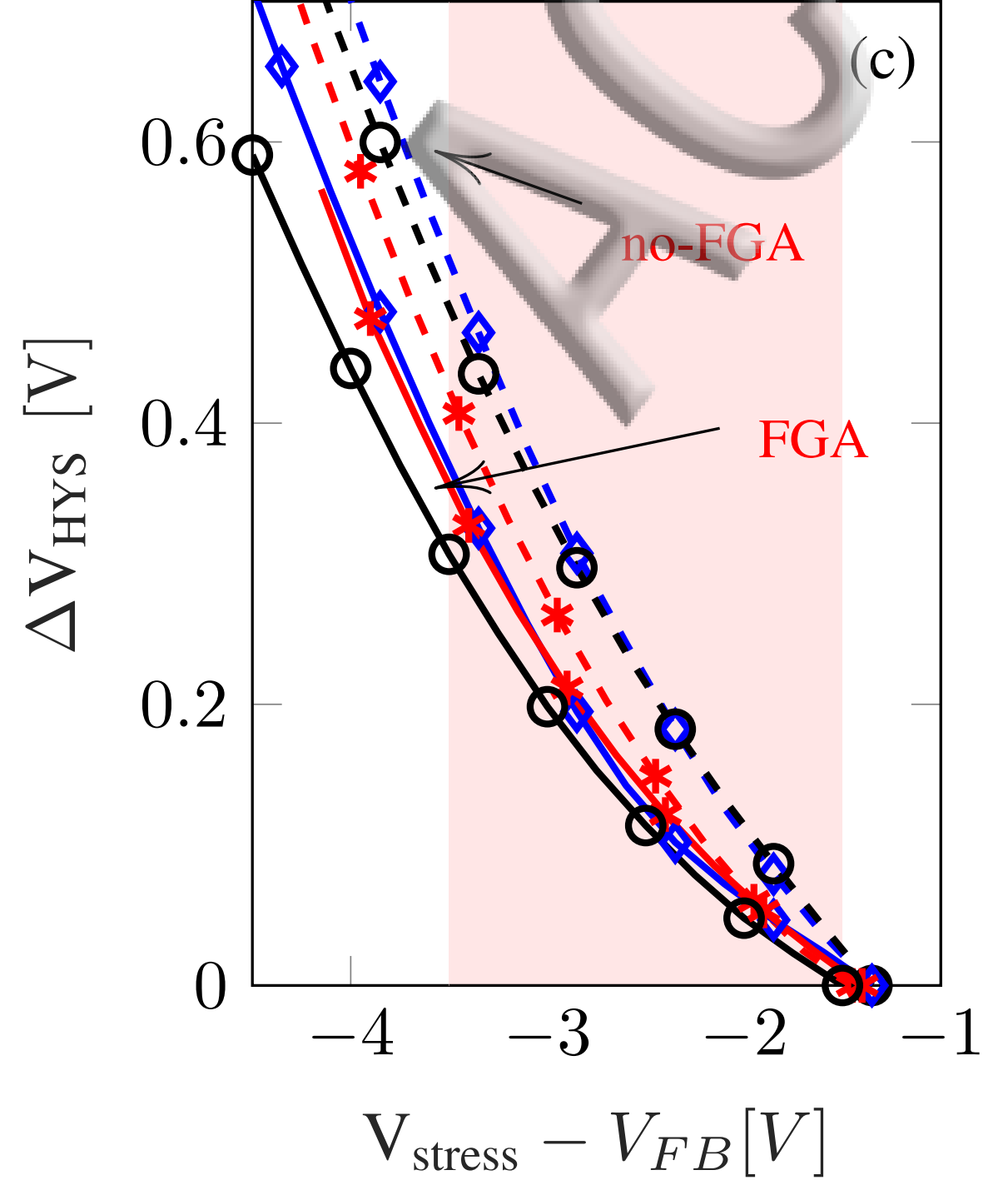

(c)
FGA
neg. stress
Freq.
200 kHz
HfO_2
C/A $[\mu F/cm^2]$
V_{gate} [V]
1.5
1
0.5
0
−4
−2
0

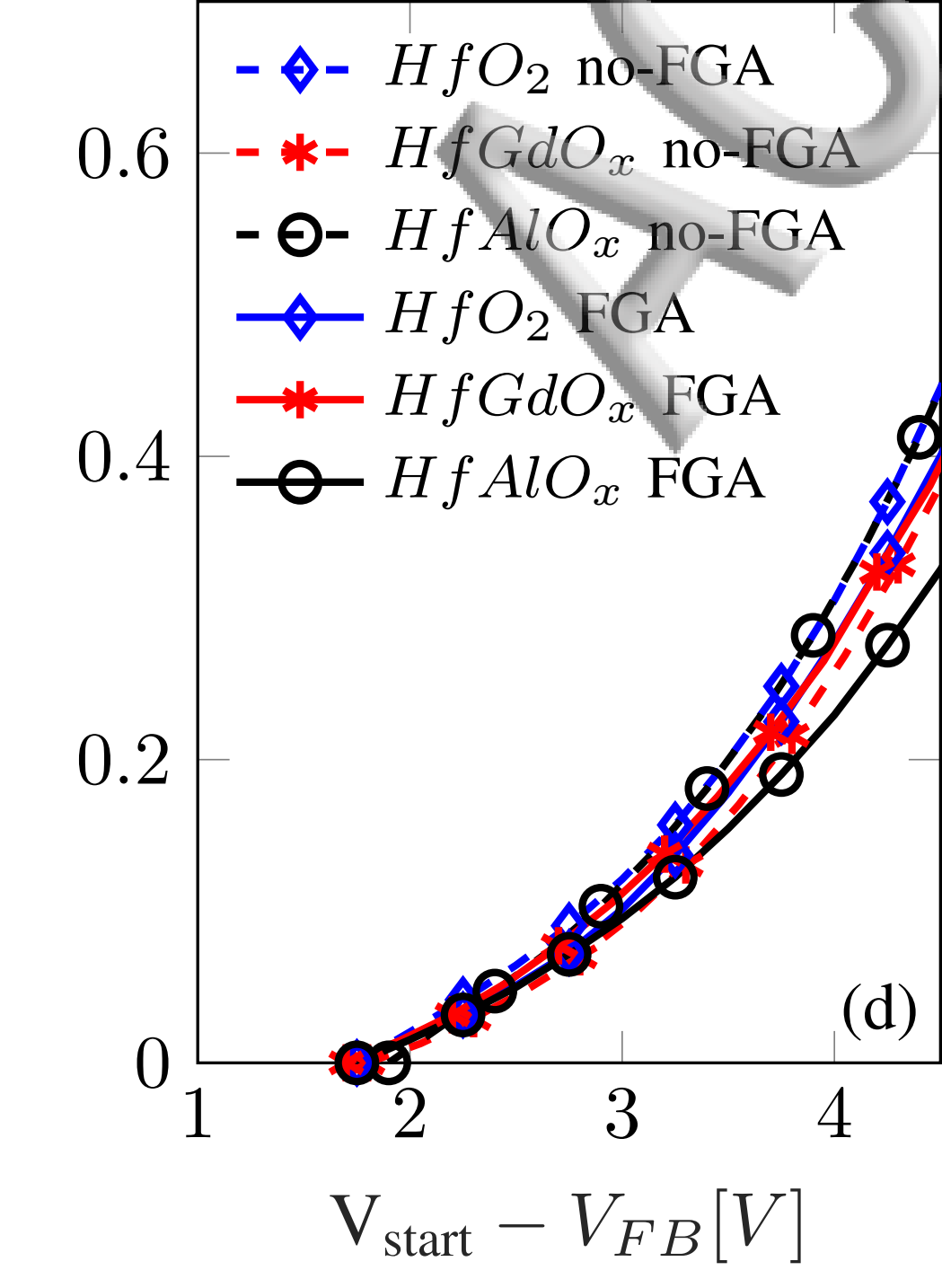

(d)
HfO_2
Freq. 200 kHz
FGA
pos. stress
$\cdot 10^{13}$
ΔD_{it} [eV^{-1}cm^{-2}]
no-FGA
FGA
HfO_2
$V_{stress} - V_{FB}$[V]
V$_{gate}$ [V]
1.5
1
0.5
0
0
2
4
−5
0
5
0.5
1

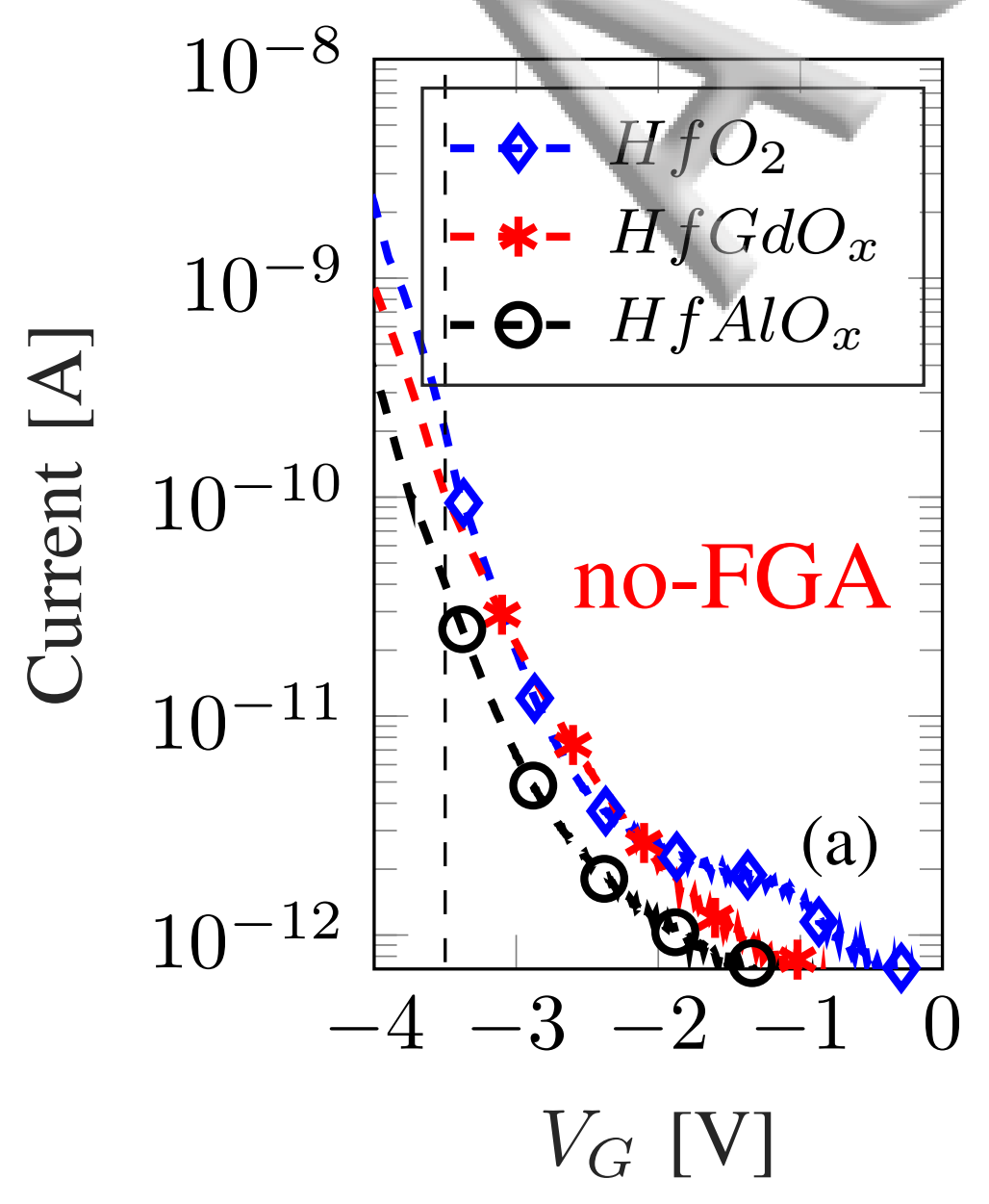

2
0
−2
−4
V_{G-} V_{FB} [V]
0
20
40
60
80
Time [Sec]
1
2
3
4
5
6
n
(e)
6° C-V, inv. to acc.
6° C-V, acc. to inv.
n^{th} C-V, inv. to acc.
n^{th} C-V, acc. to inv.
V_{start}
V_{stress_i}
Stress of ≈ 1 *sec.*
(e)

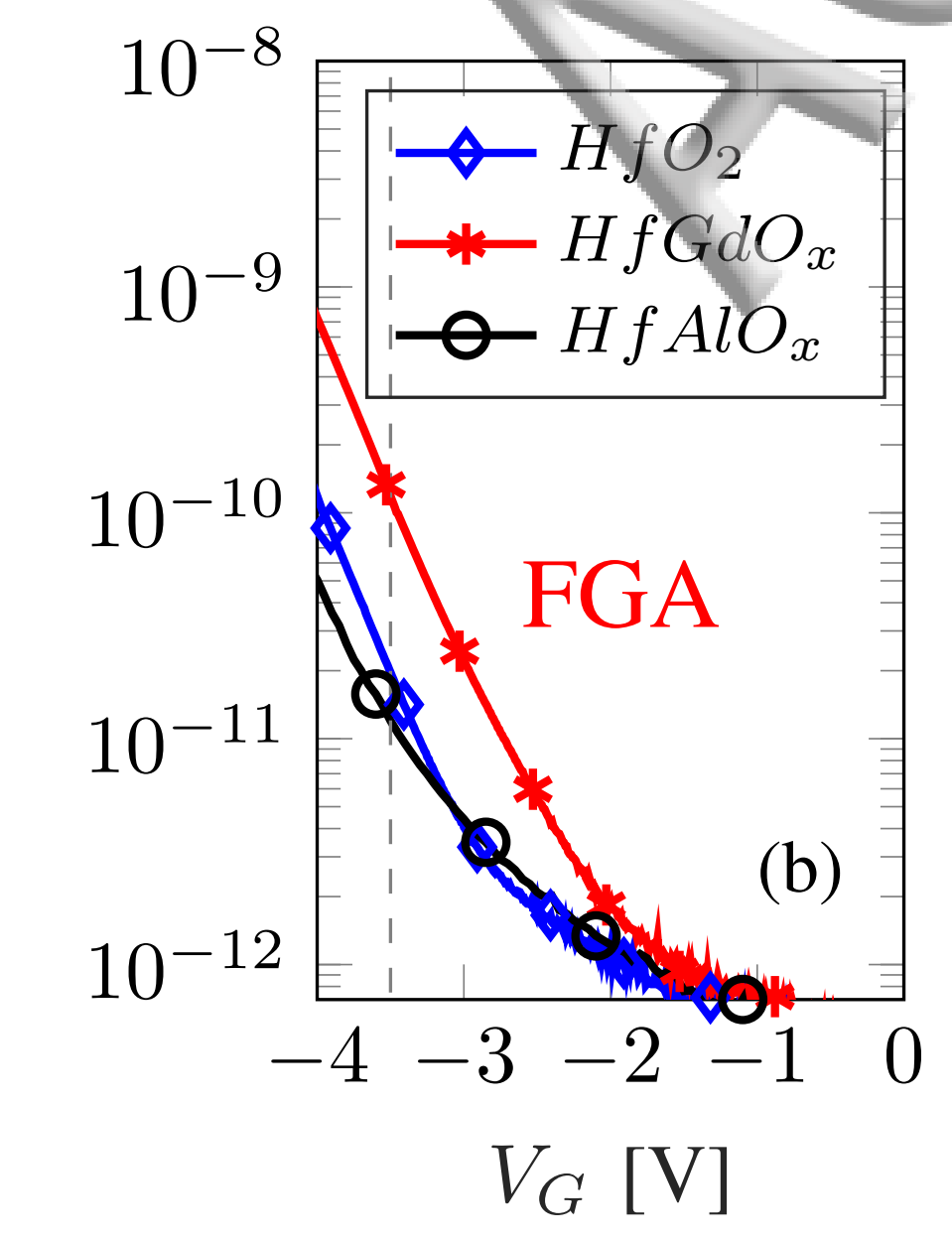

(a)
FGA
no-FGA
0
−0.2
−0.4
−0.6
−4
−3
−2
−1
ΔV_{FB} [V]
$V_{stress} - V_{FB}[V]$

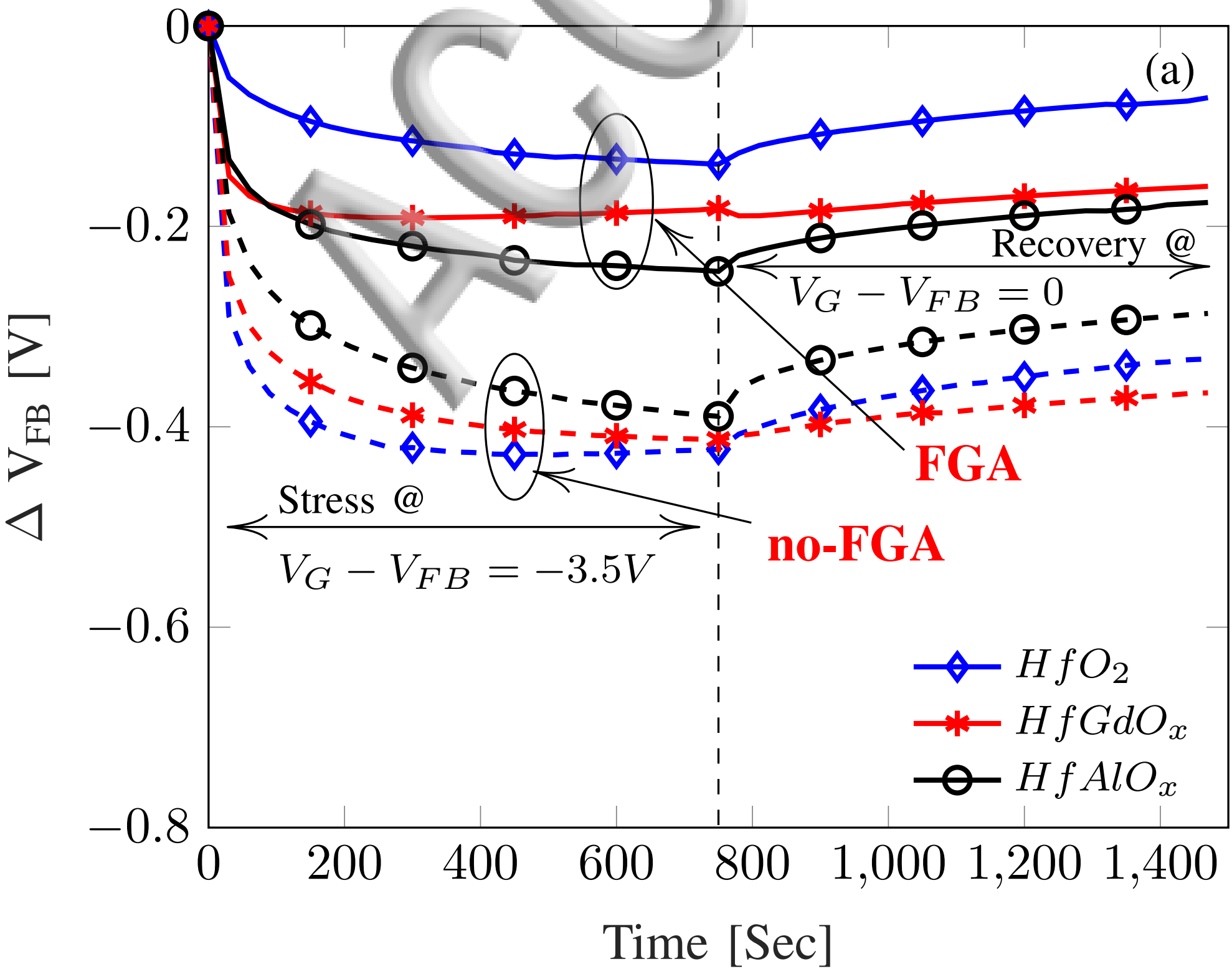

(b)
0.6
0.4
0.2
0
1
2
3
4
$V_{start} - V_{FB}[V]$

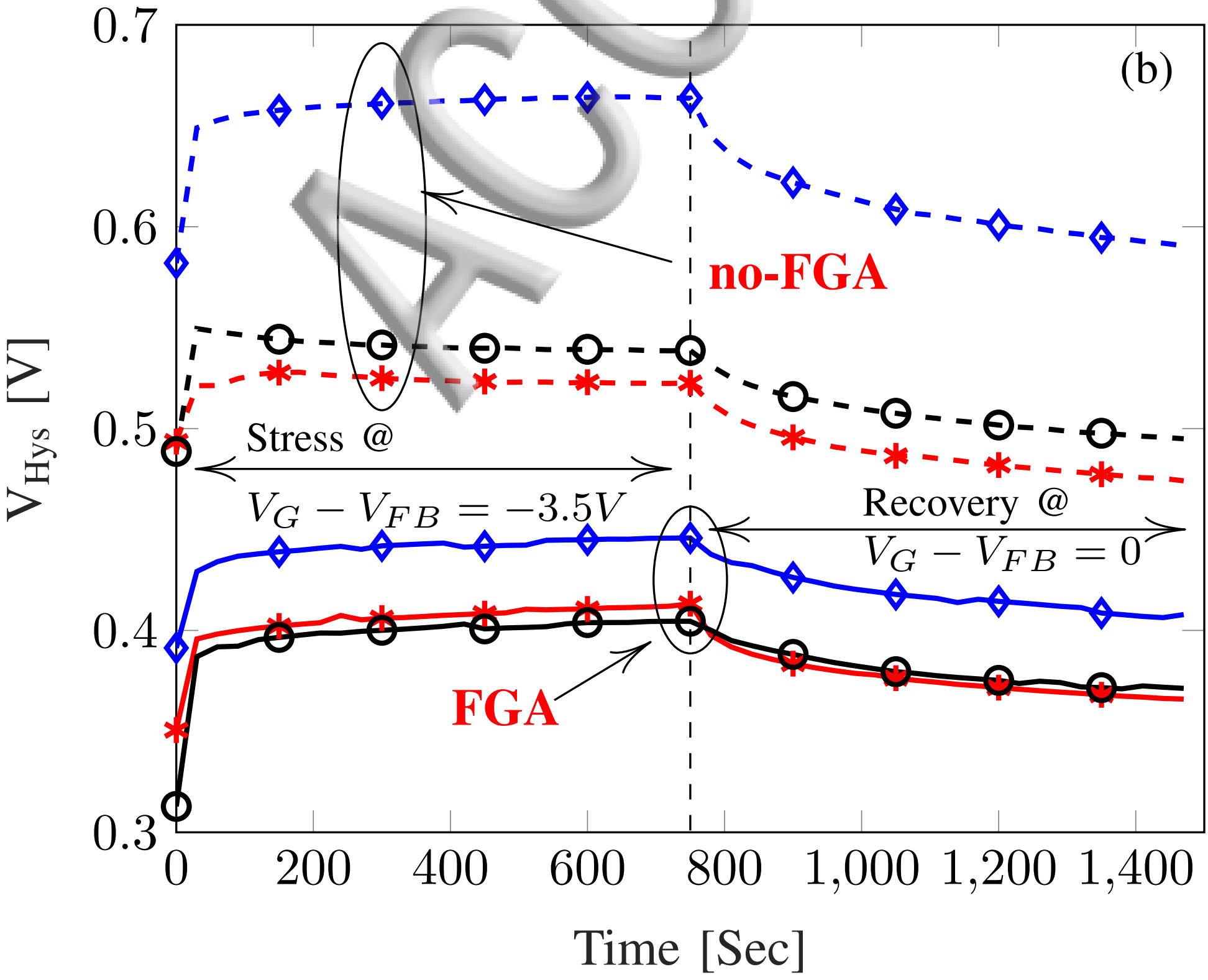

(c)
no-FGA
FGA
0.6
0.4
0.2
0
−4
−3
−2
−1
ΔV_{HYS} [V]
$V_{stress} - V_{FB}[V]$


HfO_2 no-FGA
$HfGdO_x$ no-FGA
$HfAlO_x$ no-FGA
HfO_2 FGA
$HfGdO_x$ FGA
$HfAlO_x$ FGA
0.6
0.4
0.2
0
1
2
3
4
(d)
$V_{start} - V_{FB}[V]$


10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
Current [A]
HfO_2
$HfGdO_x$
$HfAlO_x$
no-FGA
(a)
-4 -3 -2 -1 0
V_G [V]


10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
HfO_2
$HfGdO_x$
$HfAlO_x$
FGA
(b)
-4 -3 -2 -1 0
V_G [V]


(a)
0
−0.2
−0.4
−0.6
−0.8
Δ V_FB [V]
0
200
400
600
800
1,000
1,200
1,400
Time [Sec]
Recovery @
$V_G - V_{FB} = 0$
Stress @
$V_G - V_{FB} = -3.5V$
FGA
no-FGA
HfO_2
$HfGdO_x$
$HfAlO_x$


(b)
0.7
0.6
0.5
0.4
0.3
V_{Hys} [V]
no-FGA
FGA
Stress @
$V_G - V_{FB} = -3.5V$
Recovery @
$V_G - V_{FB} = 0$
0
200
400
600
800
1,000
1,200
1,400
Time [Sec]